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Two New Balanced-Input Current-Mode Differential Receivers for High-Speed Links

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***Abstract* — Two new balanced-input current-mode differential receivers for high-speed links have a low common-mode input admittance and a fairly linear differential-mode (DM) input characteristic, in addition to the linear transfer characteristic inherent to current-mode circuits. The DM input impedance may be such that no resistor is needed to reduce reflection.**

I. Introduction

A point-to-point link for high-speed binary signaling typically comprises, at the receiving end of the differential pair, a voltage-mode differential receiver and a termination consisting of a 100-Ω resistor [1]. Each terminal of the resistor is connected or ac-coupled to a conductor of the differential pair. This scheme produces a balanced-input current-sensing differential receiver. It is often used in links using low-voltage differential signaling (LVDS) or current-mode logic (CML). Here, *current-sensing* only refers to a high enough differential-mode (DM) input admittance. In the following, *current-mode* refers to a *current-mode circuit* in the meaning of circuit design [2], which implies current sensing.

There are cases where a well-defined and linear transfer (i.e., output variable versus input variable) characteristic is expected from a differential receiver for high-speed signaling, for instance in links using simultaneous bidirectional signaling and/or multilevel signaling. In such cases, the voltage-mode differential receiver might be inappropriate, but a current-mode receiver can provide a good transfer linearity and a wide bandwidth [3].

This paper is about two new balanced-input current-mode differential receivers which, like the above-mentioned scheme using a voltage-mode differential receiver, present a low common-mode (CM) input admittance. The Section II clarifies the definitions of the DM and CM input admittances. The Section III describes the new balanced-input current-mode differential receivers. The Sections IV and V discuss the input linearity of implementations using MOSFETs and BJTs, respectively.

II. Input Admittance Matrix

The input admittance matrix of the differential current-sensing receiver, denoted by $\mathbf{Y}_I$, is a 2 × 2 matrix. The input being balanced, $\mathbf{Y}_I$ is invariant when the signal input terminals are permuted, so that $\mathbf{Y}_I$ is given by

$$\mathbf{Y}_I = \begin{pmatrix} y_{I11} & y_{I12} \\ y_{I12} & y_{I11} \end{pmatrix} \tag{1}$$

If a DM input voltage v_{DM} is applied to the signal input terminals, the DM input current i_{DM} flowing through the signal input terminals is such that

$$\begin{pmatrix} i_{DM} \\ -i_{DM} \end{pmatrix} = \begin{pmatrix} y_{I11} & y_{I12} \\ y_{I12} & y_{I11} \end{pmatrix} \begin{pmatrix} v_{DM}/2 \\ -v_{DM}/2 \end{pmatrix} \tag{2}$$

Thus, the DM input admittance, denoted by y_{DM}, is given by

$$y_{DM} = \frac{i_{DM}}{v_{DM}} = \frac{y_{I11} - y_{I12}}{2} \tag{3}$$

If a CM input voltage v_{CM} is applied to the signal input terminals, the CM input current i_{CM} flowing into the signal input terminals is such that

$$\begin{pmatrix} i_{CM}/2 \\ i_{CM}/2 \end{pmatrix} = \begin{pmatrix} y_{I11} & y_{I12} \\ y_{I12} & y_{I11} \end{pmatrix} \begin{pmatrix} v_{CM} \\ v_{CM} \end{pmatrix} \tag{4}$$

Thus, the CM input admittance, denoted by y_{CM}, is given by

$$y_{CM} = \frac{i_{CM}}{v_{CM}} = 2\left(y_{I11} + y_{I12}\right) \tag{5}$$

Using (3) and (5), we find that

$$\mathbf{Y}_I = \frac{1}{4} \begin{pmatrix} y_{CM} + 4y_{DM} & y_{CM} - 4y_{DM} \\ y_{CM} - 4y_{DM} & y_{CM} + 4y_{DM} \end{pmatrix} \tag{6}$$

In the case of a low CM admittance, if y_{CM} may be regarded as equal to zero, by (6) the input admittance matrix is in the form

$$\mathbf{Y}_I = y_{DM} \begin{pmatrix} 1 & -1 \\ -1 & 1 \end{pmatrix} \tag{7}$$

which corresponds to a floating-input current-sensing receiver.

III. Balanced-Input Current-Mode Receiver

In this paper, *current mirror* always refers to a non-inverting current mirror in which the output current variation has the same orientation as the input current variation [2]. The polarity of such a current mirror may be positive or negative. The current gain of the current mirror, denoted by k, is always positive. In a positive current mirror, a positive current, denoted by I, flows into the input terminal and a positive current, equal to $k\,I$, flows into (each of) the output terminal(s). In a negative current mirror, a positive

current, denoted by I, flows out of the input terminal and a positive current, equal to $k\,I$, flows out of (each of) the output terminal(s).

The block diagram of a first balanced-input current-mode differential amplifier (DA) is shown in Fig. 1. In this circuit, the signal inputs terminals IN+ and IN− are connected to the input ports of the current mirrors M1 and M2. M1 and M2 are substantially identical and their current gain is denoted by k_{12}. The current mirror M3 is used to deliver a constant current at the common terminals of M1 and M2. M1, M2 and M3 have the same positive or negative polarity.

The current flowing into the input terminal of M3 is denoted by I_{B1}. The current gain of M3 is denoted by k_3. If the input terminals of M1 and M2 are biased by two current sources each providing a constant current I_{B2} such that

$$k_3\, I_{B1} \approx 2\,(\,k_{12} + 1)\, I_{B2} \qquad (8)$$

we see that, when the voltages of IN+ and IN− are equal, no current flows in IN+ and IN− if we assume ideal current mirror operation. Consequently, we have $y_{CM} = 0$.

An output circuit is connected to the output terminals of M1 and M2 and to the signal output terminals OUT+ and OUT−. The output circuit is such that, in the intended frequency range of operation, the difference between the output variable delivered by OUT+ and its quiescent value is substantially proportional to the difference between the current flowing into IN+ and IN−, and is substantially equal to the opposite of the difference between the output variable delivered by OUT− and its quiescent value.

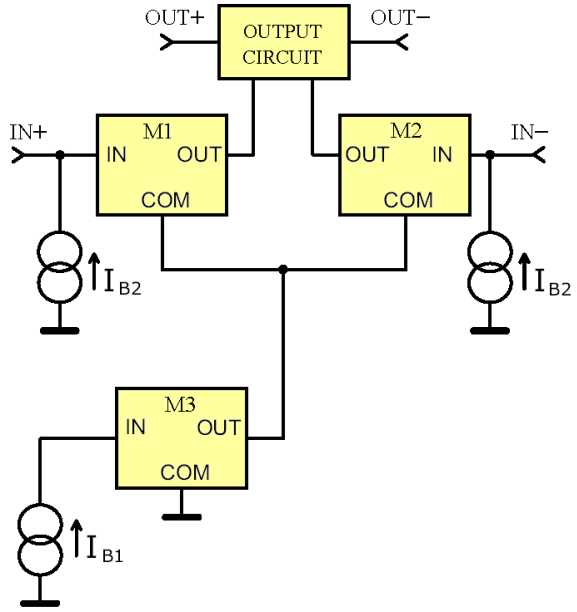

Fig. 1. A balanced-input current-mode DA.

The Fig. 2 shows a CMOS implementation of the block diagram shown in Fig. 1, using standard 2-transistor current-mirrors and series peaking inductors in the output circuit.

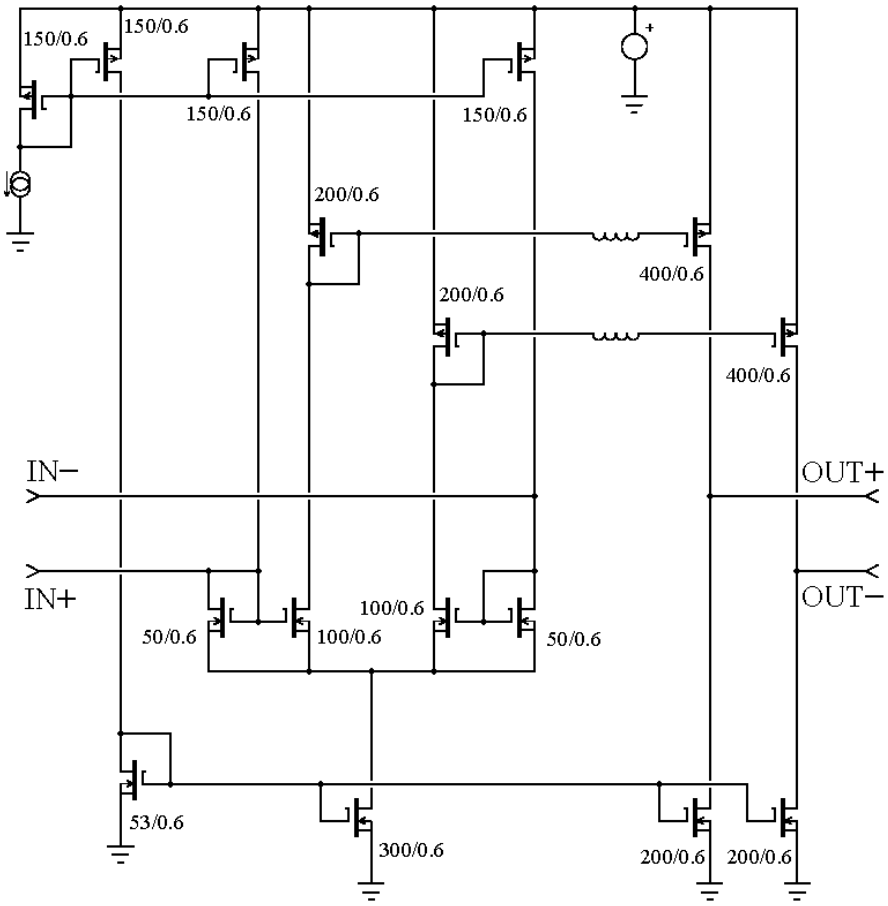

Fig 2. An implementation of the block-diagram shown in Fig. 1.

The block diagram of a second balanced-input current-mode DA is shown in Fig. 3. In this circuit, the signal input terminals IN+ and IN− are connected to the input ports of two substantially identical positive current mirrors M1 and M2, and to the input ports of two substantially identical negative current mirrors M4 and M5. The positive current mirror M3 is used to sink a constant current at the common terminals of M1 and M2, and the negative current mirror M6 is used to source the same constant current at the common terminals of M4 and M5.

We see that, in Fig. 3, when the voltages of IN+ and IN− are equal, no current flows in IN+ and IN− if we assume ideal current mirror operation. Thus, we obtain $y_{CM} = 0$. No matching is required between the floating positive current mirrors (M1, M2) and the floating negative current mirrors (M4, M5).

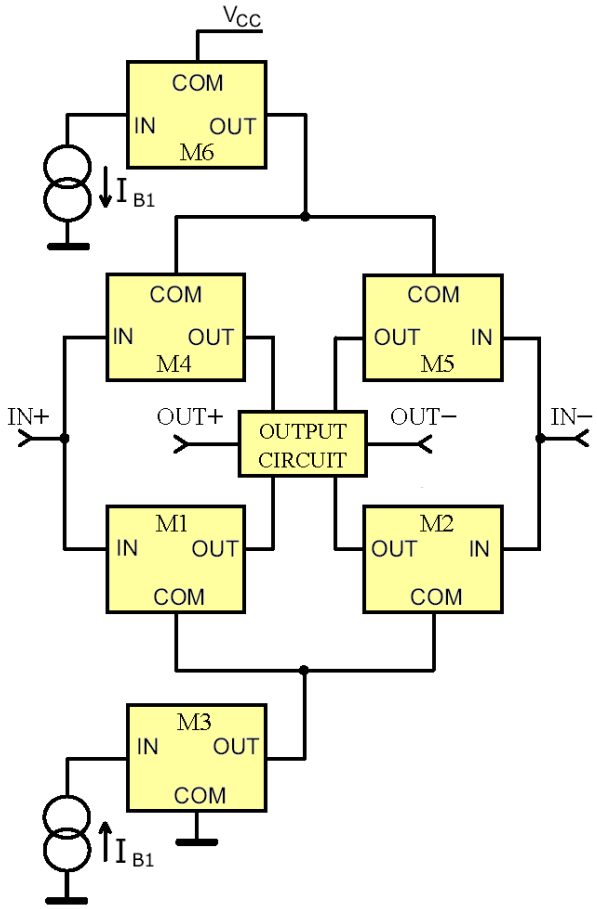

Fig. 3. A balanced-input current-mode DA.

IV. Input Linearity for MOSFET Current Mirrors

In this section, we assume that the current mirrors having their input terminal connected to IN+ and IN− are standard 2-transistor current-mirrors, built using MOSFETs operating in the saturation region. We shall use the simple device model for which the drain current i_D is given by

$$|i_D| = K' \frac{W}{2L}\left(|v_{GS}| - V_T\right)^2 \qquad (9)$$

where v_{GS} is the gate to source voltage, K' is the transconductance parameter, V_T is the threshold voltage, W is the effective channel width and L is the effective channel length. This model predicts that the CM input current is zero.

Let us assume that the same bias current, denoted by I_0, flows into the current mirror input terminals connected to IN+ and IN−. The quiescent input voltage of these current mirrors, denoted by V_0, satisfies

$$I_0 = K' \frac{W}{2L}\left(V_0 - V_T\right)^2 \qquad (10)$$

Let us use i_{IN+} and i_{IN-} to denote the currents flowing into IN+ and IN−, respectively and v_{DM} to denote the voltage between IN+ and IN−. For the circuit depicted in Fig. 1, it can be shown that the DM input current is, for $|v_{DM}| < 2|V_0 - V_T|$, exactly given by

$$i_{IN+} = i_{IN-} = K' \frac{W}{4L} v_{DM} \sqrt{4\left(V_0 - V_T\right)^2 - v_{DM}^2} \qquad (10)$$

where, K', V_T, W and L apply to the diode-connected transistors (DCTs) of M1 and M2. For the circuit shown in Fig. 3, we must add the currents produced by the DCTs of M1 and M2 to the currents produced by the DCTs of M4 and M5.

For small signals, we consequently have

$$y_{DM} = K' \frac{W}{4L} \qquad (11)$$

for the circuit shown in Fig. 1, and

$$y_{DM} = K'_N \frac{W_N}{4L_N} + K'_P \frac{W_P}{4L_P} \qquad (12)$$

for the circuit shown in Fig. 3, where K'_N, W_N and L_N apply to the n-channel input transistors of M1 and M2 and K'_P, W_P and L_P apply to the p-channel input transistors of M4 and M5. We observe that y_{DM} does not depend on I_0.

We have performed a SPICE simulation of a realization of the balanced-input current-mode DA shown in Fig. 2, using level 3 models for the standard transistors of the C5 process of AMI Semiconductor, a 0.6-µm process. In this circuit, the low-frequency current gain is about 11.9 dB (for a design value of 12.0 dB) and I_0 = 1.5 mA. The simulated input and transfer characteristics are shown in Fig. 4, where we observe a good linearity up to $|i_{IN+}| = |i_{IN-}| = 1.2$ mA. For small signals at low frequencies, the simulated DM input impedance is $z_{DM} = 1/y_{DM} \approx 545\ \Omega$. The DM input impedance predicted by (11) is about 437 Ω, in good agreement with the simulated value.

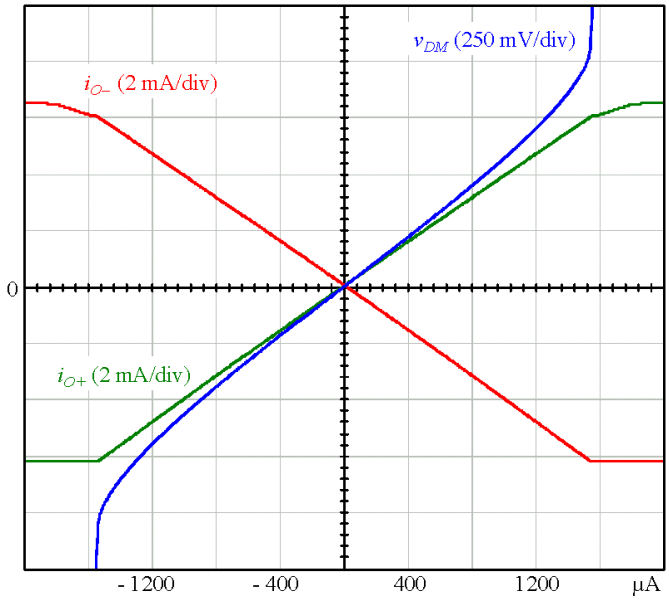

Fig. 4. DM input voltage v_{DM} and output currents i_{O+} at OUT+ and i_{O-} at OUT−, versus the DM input current i_{DM}, for the receiver shown in Fig. 2.

V. Input Linearity for BJT Current Mirrors

In this section, we assume that the current mirrors having their input terminal connected to IN+ and IN− are standard 2-transistor current-mirrors, built using BJTs operating in the forward-active mode. We will use the simple device model for which the collector current i_C is given by

$$|i_C| = I_S \left\{ e^{\frac{q|v_{BE}|-q|i_C|R_E}{k_B T}} - 1 \right\} \qquad (13)$$

where v_{BE} is the base to emitter voltage, I_S is one of the Ebers-Moll coefficients, R_E is the extrinsic emitter resistance, T is the absolute temperature, k_B is Boltzmann's constant, and q is the absolute value of electron charge such that $k_B T_0/q \approx 24{,}99$ mV at $T_0 = 290$ K. Let us again assume that the same bias current, denoted by I_0, flows into the current mirror input terminals connected to IN+ and IN−. The quiescent input voltage of these current mirrors, denoted by V_0, satisfies

$$I_0 = I_S \left\{ e^{\frac{qV_0 - qI_0R_E}{k_B T}} - 1 \right\} \qquad (14)$$

where I_S and R_E apply to the DCTs. Let us define i_{IN+}, i_{IN-} and v_{DM} as in Section IV. For the circuit shown in Fig. 1, it can be proved that the DM input current is exactly given by

$$i_{IN+} = -i_{IN-} = [I_0 + I_S] \tanh \frac{q\, v_{DM} - 2q i_{IN+} R_E}{2 k_B T} \qquad (15)$$

Thus, the wanted mode of operation is limited to $|\, i_{IN+}\,| < I_0 + I_S$, and we have

$$v_{DM} = 2 i_{IN+} R_E + \frac{2k_B T}{q} \tanh^{-1} \frac{i_{IN+}}{I_0 + I_S} \qquad (16)$$

Since in practice $I_0 >> I_S$, the wanted mode of operation is limited to $|\, i_{IN+}\,| < I_0$. For small signals, by (16) we have

$$y_{DM} \approx \frac{1}{2R_E + \dfrac{2k_B T}{qI_0}} \qquad (17)$$

For the circuit shown in Fig. 3, i_{IN+} is the sum of two terms in the form (15), the first containing the R_E for NPN DCTs, denoted by R_{EN}, and the second containing the R_E for PNP DCTs, denoted by R_{EP}. Thus, the wanted mode of operation corresponds to $|\, i_{IN+}\,| < 2I_0$ and, for small signals, we have

$$y_{DM} \approx \frac{1}{2R_{EN} + \dfrac{2k_B T}{qI_0}} + \frac{1}{2R_{EP} + \dfrac{2k_B T}{qI_0}} \qquad (18)$$

We observe that, in (17) and (18), y_{DM} can be adjusted using I_0.

We have performed a SPICE simulation of a balanced-input current-mode DA according to the block-diagram of Fig. 3, made of the standard BJTs of the UHF-1 process of Intersil. In this circuit, the low-frequency current gain is about 11.6 dB (for a design value of 12.0 dB) and $I_0 = 0.5$ mA. The simulated input characteristic is shown in Fig. 5. We observe a good linearity up to $|\, i_{IN+}\,| = |\, i_{IN-}\,| = 0.6$ mA. The DM input impedance predicted by (18) is about 60.2 Ω, which agrees reasonably well with the value $z_{DM} = 1/y_{DM} \approx 75.7$ Ω provided by the simulation. We also find that (15) gives an interesting estimate of the non-linearity, since it predicts that $|\, i_{IN+}\,| = |\, i_{IN-}\,|$ should saturate at $2I_0 = 1$ mA whereas the simulated value is about 0.9 mA.

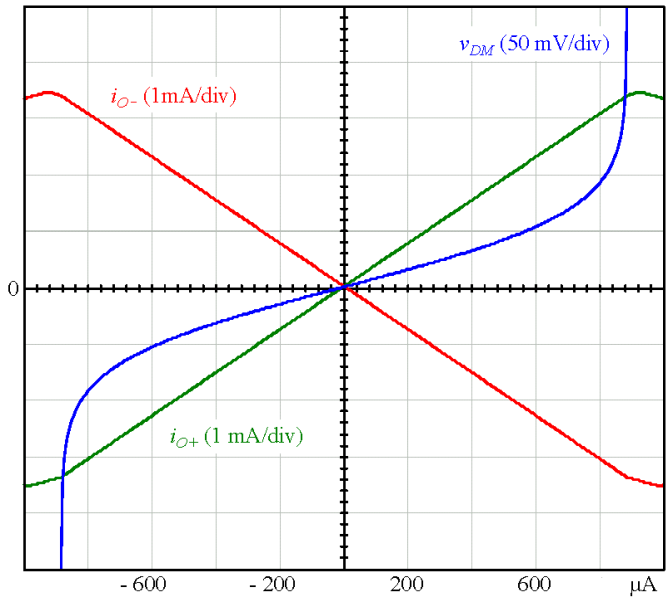

Fig. 5. DM input voltage v_{DM} and output currents i_{O+} at OUT+ and i_{O-} at OUT−, versus the DM input current i_{DM}, for a receiver built using BJTs, according to Fig. 3.

VI. Conclusion

Two new balanced-input current-mode differential receivers for high-speed links have been defined. Unlike most current-mode DAs, they provide a low CM input admittance. They also offer a fairly linear DM input characteristic, in addition to the linear transfer characteristic inherent to current-mode circuits. Since it is possible to obtain $z_{DM} = 1/y_{DM} \approx 100$ Ω, this type of receiver may effectively absorb an incoming signal from a differential pair having a characteristic impedance of 100 Ω. This eliminates the need for an on-chip or off-chip termination.

The circuits discussed in this paper can be compared with the much more complex translinear input stage of the current-mode op-amp introduced by Toumazou and Lidgey [2, § 4.8.4] [4].

References

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