

A differential audio input amplifier using a bootstrapped power supply

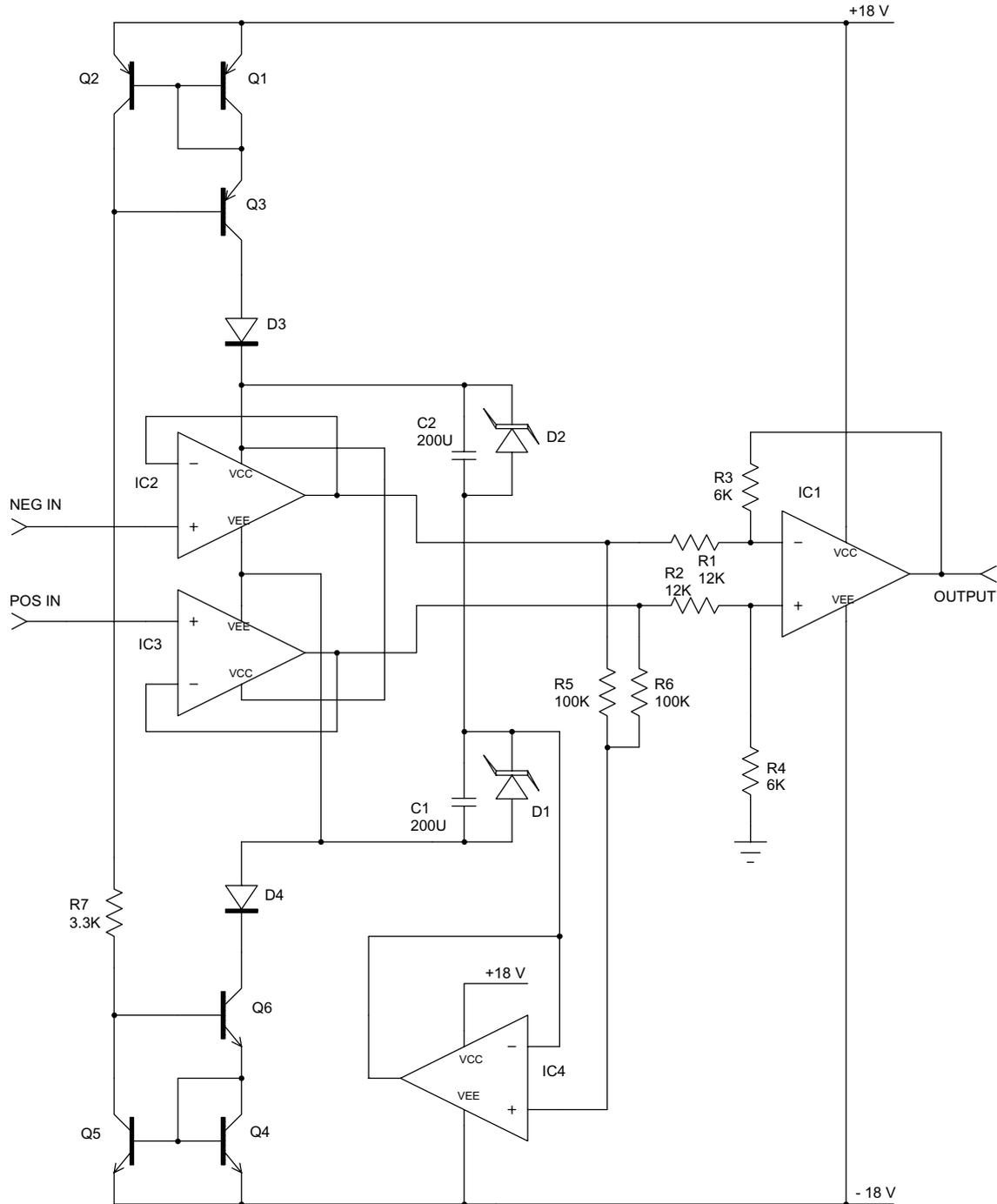


Fig. 1. Principle of the differential audio input amplifier

Table of contents

	page
1. Scope	2
2. Discussion of a classic differential amplifier	2
3. Problem to be solved	4
4. Description of the differential audio input amplifier	5
5. References	6
Annex A	A-1 to A-11
Annex B	B-1 to B-11
Annex C	C-1 to C-2

This research note has 30 pages including annexes.

1. Scope

This research note describes a differential audio input amplifier using a bootstrapped power supply, having inputs presenting a low common-mode admittance and extended differential-mode and common-mode voltage ranges. This innovative differential audio input amplifier was disclosed in a patent of France [1] filed in 2002, and later implemented in the balanced audio inputs of a digital loudspeaker processor, the NX242 Digital TDcontroller of Nexco [2]-[3].

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2. Discussion of a classic differential amplifier

A schematic diagram of a classic differential amplifier using a single operational amplifier is shown in Fig. 2.

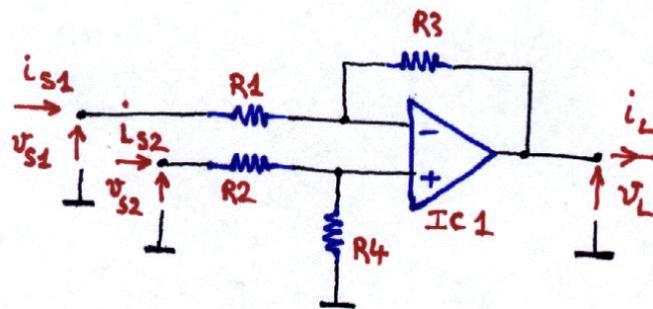


Fig. 2. A classic differential amplifier

For this circuit, assuming a very large gain of the operational amplifier IC1, the input impedance matrix with respect to ground is

$$\mathbf{Z}_{in} = \begin{pmatrix} R_1 & R_4 \\ 0 & R_2 + R_4 \end{pmatrix} \quad (1)$$

and the output voltage is

$$v_L = \frac{R_4(R_1 + R_3)}{R_1(R_2 + R_4)} v_{S2} - \frac{R_3}{R_1} v_{S1} \quad (2)$$

When most of the present work was performed (in 2002), two popular high-performance differential line receivers were proposed by Analog Devices, the SSM2141 and the SSM 2143. Both are now (in 2025) obsolete. In the case of the SSM2143 differential line receiver integrated circuit, the nominal resistance values [4] are $R_1 = R_2 = 12 \text{ k}\Omega$ and $R_3 = R_4 = 6 \text{ k}\Omega$. In the case of the SSM2141 differential line receiver integrated circuit, the nominal resistance values [5] are $R_1 = R_2 = 25 \text{ k}\Omega$ and $R_3 = R_4 = 25 \text{ k}\Omega$.

If $R_1 = R_2$ and $R_3 = R_4$, the output voltage of the classic differential amplifier is

$$v_L = G (v_{S2} - v_{S1}) \quad (3)$$

with a nominal gain

$$G = \frac{R_4}{R_1} = \frac{R_3}{R_1} \quad (4)$$

so that the nominal gain is $G = 0.5$ for the nominal resistance values of the SSM2143, and $G = 1.0$ for the nominal resistance values of the SSM2141.

According to (3), the classic differential amplifier perfectly rejects the open-circuit common-mode voltage of a 2-port generator having a null internal impedance matrix with respect to ground. If the classic differential amplifier has its inputs connected to a 2-port generator of internal impedance matrix

$$\mathbf{Z}_{out} = \begin{pmatrix} Z_{out1} & 0 \\ 0 & Z_{out2} \end{pmatrix} \quad (5)$$

with respect to ground, we have

$$v_L = \frac{R_4(R_1 + R_3 + Z_{out1})}{(R_1 + Z_{out1})(R_2 + R_4 + Z_{out2})} e_{S2} - \frac{R_3}{R_1 + Z_{out1}} e_{S1} \quad (6)$$

where e_{S1} and e_{S2} are the open-circuit voltages of the 2-port generator, corresponding to the generator terminal connected to R_1 and the generator terminal connected to R_2 , respectively. Thus, if $R_1 = R_2$, $R_3 = R_4$ and $Z_{out1} = Z_{out2}$, the output voltage is

$$v_L = G' (e_{S2} - e_{S1}) \quad (7)$$

with a nominal gain

$$G' = \frac{R_4}{R_1 + Z_{out1}} = \frac{R_3}{R_1 + Z_{out2}} \quad (8)$$

so that the output voltage only depends on the open-circuit differential-mode voltage $e_{S2} - e_{S1}$, the open-circuit common-mode voltage $(e_{S1} + e_{S2})/2$ being consequently perfectly rejected.

However, it follows from (6) that the rejection of an open-circuit common-mode voltage $(e_{S1} + e_{S2})/2$ by this circuit is very sensitive to an impedance imbalance of the 2-port generator, that is to say on any difference between Z_{out1} and Z_{out2} . Worse, (1) tells us that the input of the classic differential amplifier is

not a symmetric passive 2-port (the input impedance matrix is not the same if the two ports are exchanged), and not even a reciprocal 2-port (the input impedance matrix is not symmetric). For these reasons, the input of the classic differential amplifier is not a balanced input (according to the definition provided in § 5.2 of [6]).

A curious consequence of the fact that the input of the classic differential amplifier is neither a symmetric passive 2-port nor a reciprocal 2-port is the following: if this differential amplifier has its input connected to a floating source, therefore with $i_{S2} = -i_{S1}$, it follows from (1) that:

$$\begin{cases} v_{S1} = (R_4 - R_1) i_{S2} \\ v_{S2} = (R_2 + R_4) i_{S2} \end{cases} \quad (9)$$

Accordingly, for the nominal resistance values of the SSM2141, we have $v_{S1} = 0$. This effect is well known (see for instance § 4 of [7]). This effect is not as bad in the case of the nominal resistance values of the SSM2143, for which $v_{S1} / v_{S2} = -1/3$.

According to the § 14.5.2.2.1 of [8], the nominal input impedance of an audio input should be measured using a floating source. According to (9), the nominal input impedance seen by a floating generator is

$$Z_{in \text{ float}} = \frac{v_{S2} - v_{S1}}{i_{S2}} = R_1 + R_2 \quad (10)$$

which takes on the values 24 k Ω in the case of the nominal resistance values of the SSM2143 and 50 k Ω in the case of the nominal resistance values of the SSM2141.

Outputs intended to be possibly connected to the differential audio inputs of a digital loudspeaker processor, such as mixer outputs, may deliver levels up to 28 dBu, typically [9]. Experience shows that a loudspeaker processor is likely to be used in configurations where a common-mode voltage of several volts r.m.s is present at its inputs. Since 28 dBu represent about 55 V peak-to-peak between the inputs, and about 27.5 V peak-to-peak at each input, a SSM2141 cannot be used. The 28 dBu headroom of the SSM2143 used with a ± 15 V supply voltage might seem suitable. However, considering a typical input voltage range of ± 15 V for this circuit [4], this leaves only 2.5 V peak-to-peak for the common-mode (signal unbalance + noise) voltage. What is the purpose of providing 90 dB of common-mode rejection, if the signal starts to clip with 0.88 V r.m.s of common-mode voltage? Note that the SSM2143 is not completely specified for any power supply voltage other than ± 15 V, even though its absolute maximum power supply voltage is ± 18 V.

The clipping issue of the SSM2143 is not present with an INA137 audio differential line receiver used to obtain a gain of 1/2. This is because the INA137 is fully specified at a power supply voltage of ± 18 V, in which case it has a guaranteed common-mode voltage range of ± 46.5 V [10]. The INA137 is currently (in 2025) available from Texas Instruments.

3. Problem to be solved

If an INA137 is used for the differential audio inputs of a digital loudspeaker processor, the remaining problem to be solved is that this classic differential amplifier neither has a balanced input nor an input presenting a low common-mode admittance. This could conceptually be solved by connecting the positive input of the classic differential amplifier to the output of a first unity gain amplifier, and the negative input of the classic differential amplifier to the output of a second unity gain amplifier. If the unity gain amplifiers are used in a conventional configuration, this solution does not work, because:

- each operational amplifier used as a follower will introduce a clipping problem for a high differential-mode voltage of 55 V peak-to-peak combined with a significant common-mode voltage; and
- each operational amplifier used as a follower is likely to somewhat degrade the common-mode rejection of the circuit (see § 5.15.1, page 359 of [11]).

It is useful to note that, in practice, a “significant common-mode voltage” is typically mostly a periodic signal comprising the power frequency and some of its harmonics. To clarify the wanted characteristics of a differential audio input, we wish it to: present a common-mode admittance less than or equal to 2 μS in the audio range; operate normally with a differential input signal level of up to +28 dBu; and be such that the nominal common-mode rejection ratio of 80 dB is guaranteed, possibly in the presence of a differential-mode input signal of up to +28 dBu, at a common-mode level of up to 3 V r.m.s from DC to 40 kHz, and of up to 7 V r.m.s. from 45 Hz to 400 Hz.

4. Description of the differential audio input amplifier

A schematic diagram presenting the principle of the differential audio input amplifier that we want to discuss is shown in Fig. 1 (see page 1 above). In Fig. 1, the input terminals of the differential audio input amplifier are “POS IN” and “NEG IN”. In this differential audio input amplifier, the input signals of a classic differential amplifier (composed of IC1 and R1 to R4 in Fig. 1, as in Fig. 2) are the output signals of a front-end circuit composed of everything but IC1 and R1 to R4 in Fig. 1. In the example shown in Fig. 1, the gain of the differential amplifier is 1/2.

The use of a front-end circuit comprising two floating power supplies was well known when the differential audio input amplifier was introduced, see for instance § 2.4.3 and Fig. 2.22 of [12]. This configuration was also referred to as “bootstrapped power supply”, see for instance pages 284 and 285 of [13], a similar material being proposed in page 359 of [11]. The front-end of the differential audio input amplifier shown in Fig. 1 is simply a dual follower using a bootstrapped power supply, in which the floating power supplies have been replaced by two capacitors (C1 and C2) each connected in parallel with a voltage regulation diode (D1 or D2) and power fed using a suitable Wilson current mirror.

The differential audio input amplifier shown in Fig. 1 solves the problem explained in § 3 above, because:

- each operational amplifier used as a follower will not introduce a clipping problem for a high differential-mode voltage of 55 V peak-to-peak combined with a reasonable common-mode voltage; and
- each operational amplifier used as a follower will not significantly degrade the common-mode rejection of the circuit, because it will not see the common-mode voltage at its positive input.

It is worth noting that this differential audio input amplifier has two mode operation: in “mode A”, which occurs at low enough common-mode voltages, the diodes D3 and D4 are always forward biased; in “mode B”, which occurs at high enough common-mode voltages, the diodes D3 and D4 are sometimes reverse biased.

Annex A shows a first SPICE simulation of a possible implementation of the differential audio input amplifier, in which the voltage applied to each input comprises a 4.25 V peak common-mode component (3 V r.m.s.) at 50 Hz and a 27.52 V peak differential-mode component (to obtain a +28 dBu differential mode input) at 230 Hz. According to the figure of page A-10, the circuit of Annex A operates in mode A. Annex B shows a second SPICE simulation of the same implementation of the differential audio input amplifier, in which the voltage applied to each input comprises a 9.90 V peak common-mode component (7 V r.m.s.) at 50 Hz and the same 230 Hz and 27.52 V peak differential-mode component as in Annex A. According to the figure of page B-10, the circuit of Annex B operates in mode B. A comparison of the

figures of pages A-9 and B-9 shows that the power supply voltage of the operational amplifiers IC2 and IC3 of Fig. 1 varies more in mode B than in mode A. A comparison of the figures of pages A-11 and B-11 shows that the output of the operational amplifier IC4 of Fig. 1 must supply a much higher current in mode B than in mode A.

Annex C shows the schematic diagram of one of the analog front-ends of a prototype of the NX242 Digital TDcontroller of Nexo, in which the differential audio input amplifier is implemented, the input terminals being labeled “Input +” and “Input –”. This schematic diagram does not include the input protection circuits. Z1201 is a copper trace creating a connection to ground, used to create a wanted ground structure, in addition to a ground plane below the circuit parts. The input biasing resistors R1218 and R1219 are parts of a bootstrap circuit also comprising C1211 and R1220, to decrease the common-mode admittance at audio frequencies, in a manner similar to what is shown in Fig 3.14, page 99 of [13]. In the analog front-end of Annex C, it seems that the tolerance requirement of 0.1 % for R1221 and R1222 is not reasonable.

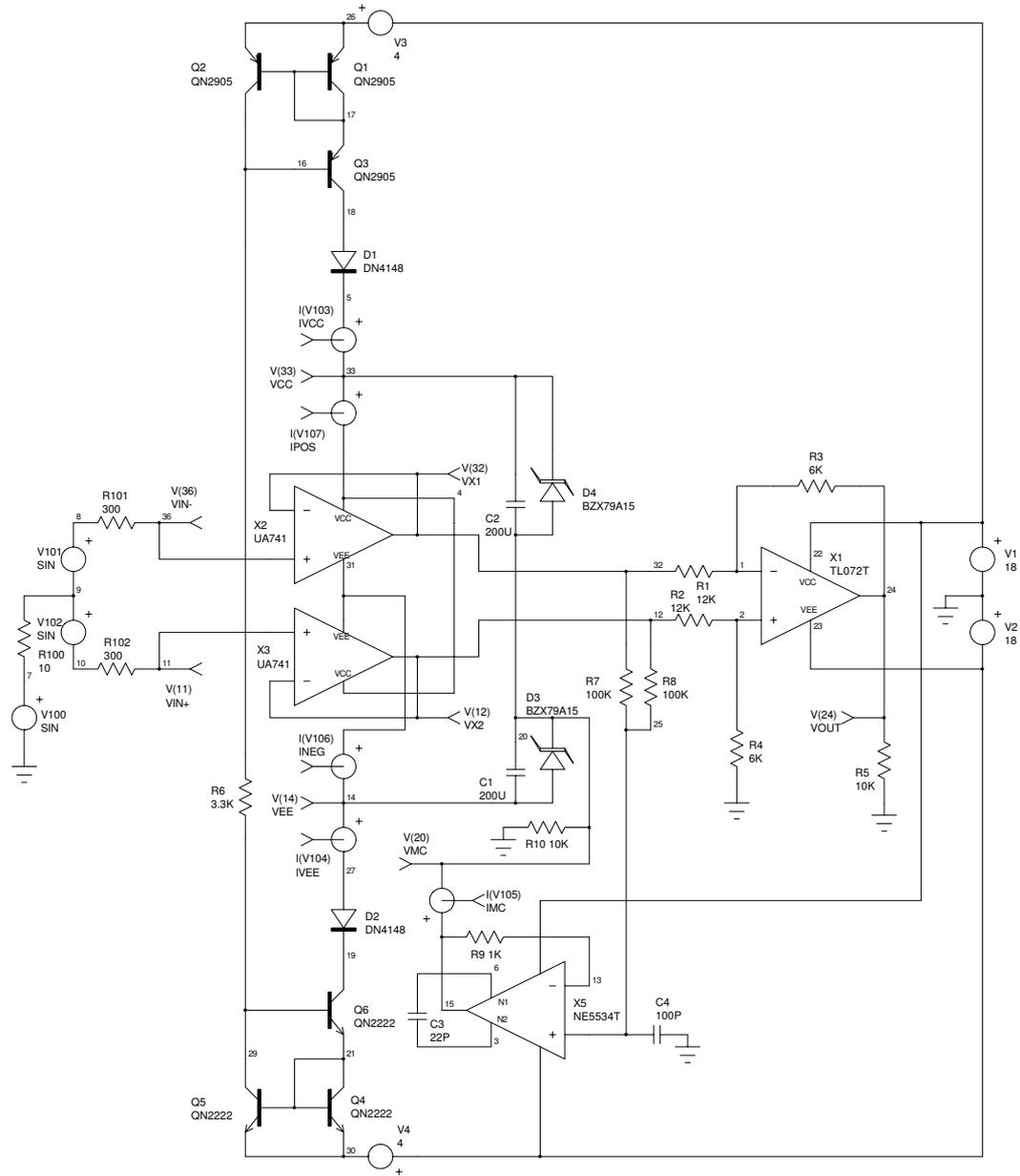
5. References

- [1] French patent application FR0207888 of 25 June 2002. Title: *Procédé et dispositif pour la réception de signaux différentiels avec une forte réjection du mode commun*. Inventors: Frédéric Broydé and Evelyne Clavelier. Publication number FR2841408B1. Patent granted to Excem on 5 May 2006.
- [2] *NX242 Digital Digital TDcontroller — User Manual*, load2_22, Nexo, 2004.
- [3] *NX242 Digital Digital TDcontroller — Service Manual*, rev100606, Nexo, 2006.
- [4] *SSM2143, –6 dB Differential Line Receiver*, data sheet Analog Devices, Rev. A, 2011.
- [5] *SSM2141, High Common-Mode Rejection Differential Line Receiver*, data sheet Analog Devices, Rev. C, 2007.
- [6] IEC 60268-2:1987. Sound system equipment - Part 2: Explanation of general terms and calculation methods.
- [7] B. Whitlock, “Balanced Lines in Audio Systems: Fact, Fiction, and Transformers”, *J. Audio Eng. Soc.*, Vol.43, No. 6, June 1995, pp. 454-464.
- [8] IEC 60268-3:2001. Sound system equipment - Part 3: Amplifiers.
- [9] 1202-VLZ pro 12-channel mic/line mixer — Owner’s Manual, Mackie Designs, Inc, part No. 820-028-01 Rev B 02/2000.
- [10] *INA137, INA2137 — Audio Differential Line Receiver $\pm 6\text{dB}$ ($G= 1/2$ or 2)*, data sheet Burr-Brown PDS-1391B, 1997.
- [11] P. Horowitz, W. Hill, *The Art of Electronics*, Third Edition, Cambridge University Press, 2015.
- [12] J.G. Graeme, *Applications of Operational Amplifiers — Third-Generation Technique*, New York: McGraw-Hill, 1973.
- [13] P. Horowitz, W. Hill, *The Art of Electronics* (First Edition), Cambridge University Press, 1980.

ANNEX A

SPICE simulation of a differential audio input amplifier

(simulation *input7.cir*)



INPUT 7

```

E:\SPICE4\NEXO\INPUT7
*SPICE_NET
*INCLUDE TIA.LIB
.SUBCKT TL072T      1 2 3 4 5
*
C1      11 12 3.498E-12
C2       6  7 15.00E-12
DC       5 53 DX
DE       54  5 DX
DLP      90 91 DX
DLN      92 90 DX
DP        4  3 DX
EGND    99  0 POLY(2) 3 0 4 0 0 .5 .5
FB       7 99 POLY(5) VB VC VE VLP VLN 0 4.715E6 -5E6 5E6 5E6 -5E6
GA       6  0 11 12 282.8E-6
GCM      0  6 10 99 8.942E-9
ISS      3 10 DC 195.0E-6
HLIM    90  0 VLIM 1K
J1       11  2 10 JX
J2       12  1 10 JX
R2        6  9 100.0E3
RD1      4 11 3.536E3
RD2      4 12 3.536E3
RO1      8  5 150
RO2      7 99 150
RP        3  4 2.143E3
RSS     10 99 1.026E6
VB        9  0 DC 0
VC        3 53 DC 2.200
VE       54  4 DC 2.200
VLIM     7  8 DC 0
VLP     91  0 DC 25
VLN      0 92 DC 25
.MODEL DX D(IS=800.0E-18)
.MODEL JX PJF(IS=15.00E-12 BETA=270.1E-6 VTO=-1)
.ENDS
.TRAN 50U 50M 0 50U
*INCLUDE NONLIN.LIB
.SUBCKT UA741 2      3 6 7 4
*
- IN + OUT VCC VEE
*
QNI1 10 2 13 QNI1
QNI2 12 3 13 QNI2
.MODEL QNI1 NPN(NF=1.5 BF=111 IS=8E-16 CJE=3PF)
.MODEL QNI2 NPN(NF=1.5 BF=144 IS=8.3E-16 CJE=3PF)
Q3 13 14 4 QN741
IEE 4 14 185NA
CCM 13 4 2.5PF
RCM 13 4 10MEG
RC1 11 10 1K
RC2 11 12 1K
CHF 10 12 55PF
D1 7 11 D741
RP 7 4 10K
GA 0 15 12 10 .9MMHO
GCM 0 15 13 0 6.3NMHOS
R2 15 0 100K
D2 15 0 D741
D3 0 15 D741
C2 15 16 30PF
GB 16 0 15 0 12.5
RO2 16 0 1000
D4 16 17 D741P
EP 17 0 7 0 -1.8 1
D5 18 16 D741P
EN 0 18 0 4 -2.3 1
.MODEL D741P D(RS=1M)

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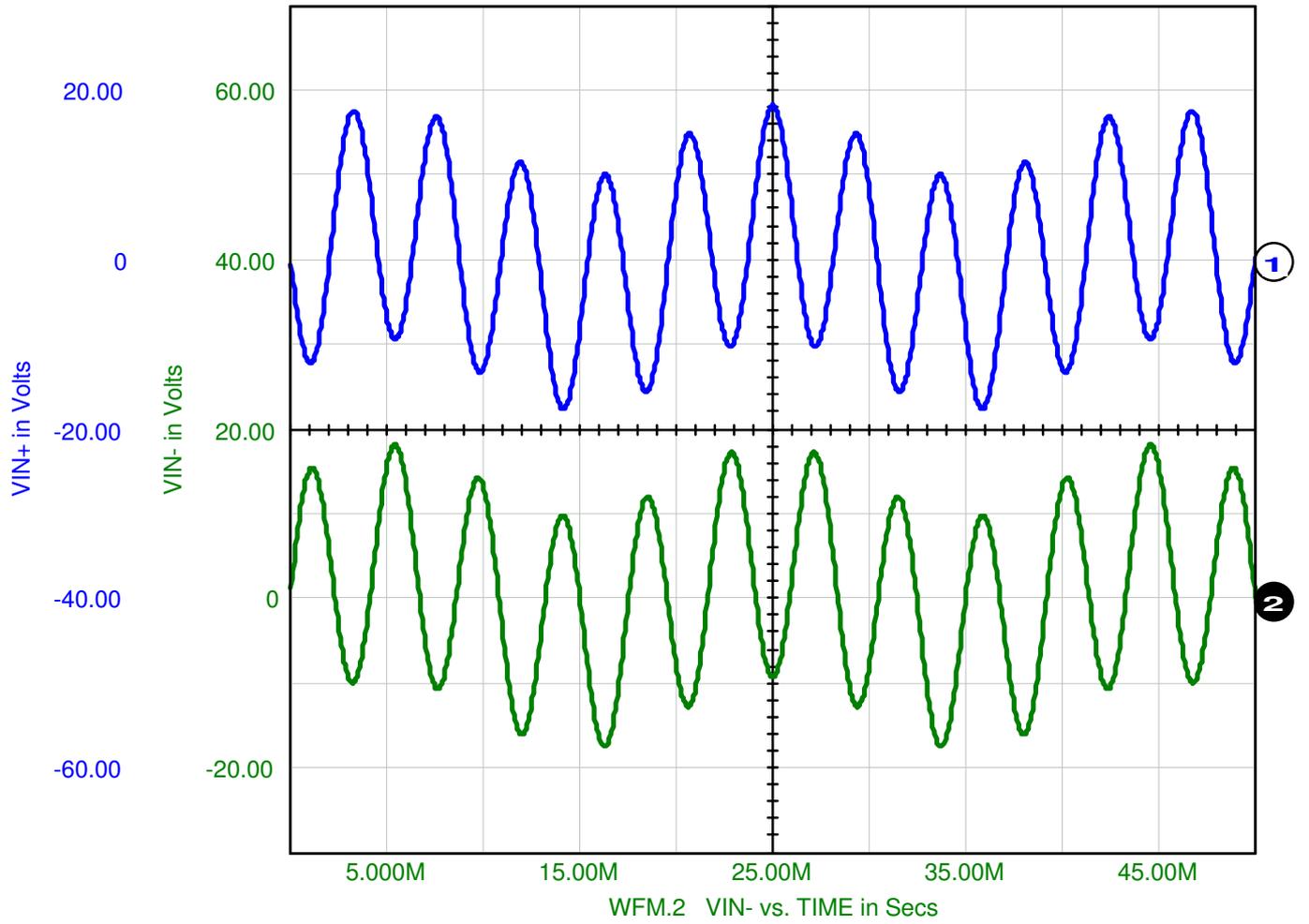
D6 19 16 D741
D7 16 20 D741
IRO 20 19 170UA
RR0 16 21 1MEG
Q4 7 19 21 QNO
Q5 4 20 21 QPO
.MODEL QNO NPN (BF=150 CJC=3P IS=1E-14)
.MODEL QPO PNP (BF=150 CJC=3P IS=1E-14)
L1 21 6 30UHY
RL1 21 6 1K
.MODEL D741 D (CJO=3PF)
.MODEL QN741 NPN
.ENDS
*INCLUDE BJTP.LIB
.MODEL QN2905 PNP (IS=3.81E-13 NF=1.0 BF=260 VAF=114
+ IKF=3.6E-01 ISE=5.85E-11 NE=2.0 BR=4 NR=1.0 VAR=20
+ XTB=1.5 RE=1.2E+00 RB=4.8E+00 RC=4.8E-01
+ CJE=4.6E-11 CJC=1.9E-11 TF=7.9E-10 TR=2.1E-08)
* 40 VOLT 0.60 AMP 200 MHZ SIPNP TRANSISTOR 08-06-1990
*INCLUDE DEVICE.LIB
.MODEL DN4148 D (RS=.8 CJO=4PF IS=7E-09 N=2 VJ=.6V
+ TT=6E-09 M=.45 BV=100V)
.MODEL QN2222 NPN (IS=1.9E-14 BF=150 VAF=100 IKF=.175 ISE=5E-11 NE=2.5
+ BR=7.5 VAR=6.38 IKR=.012 ISC=1.9E-13 NC=1.2 RC=.4 XTB=1.5
+ CJE=26PF TF=.5E-9 CJC=11PF TR=30E-9 KF=3.2E-16 AF=1.0)
*INCLUDE DIODE.LIB
.MODEL BZX79A15 D (RS=8.7297 BV=14.927
+ CJO=578.05P TT=20N N=2 IS=3.8E-09 IBV=1M)
* PHILIPS 15 VOLT ZENER
.OPTION ITL1=1000 METHOD=GEAR
*INCLUDE TI.LIB
.SUBCKT NE5534T 1 2 3 4 5 6 7
*
C1 11 12 7.703E-12
DC 5 53 DX
DE 54 5 DX
DLP 90 91 DX
DLN 92 90 DX
DP 4 3 DX
EGND 99 0 POLY(2) 3 0 4 0 0 .5 .5
FB 7 99 POLY(5) VB VC VE VLP VLN 0 2.893E6 -3E6 3E6 3E6 -3E6
GA 6 0 11 12 1.382E-3
GCM 0 6 10 99 13.82E-9
IEE 10 4 DC 133.0E-6
HLIM 90 0 VLIM 1K
Q1 11 2 13 QX
Q2 12 1 14 QX
R2 6 9 100.0E3
RC1 3 11 723.3
RC2 3 12 723.3
RE1 13 10 329
RE2 14 10 329
REE 10 99 1.504E6
RO1 8 5 50
RO2 7 99 25
RP 3 4 7.757E3
VB 9 0 DC 0
VC 3 53 DC 2.700
VE 54 4 DC 2.700
VLIM 7 8 DC 0
VLP 91 0 DC 38
VLN 0 92 DC 38
.MODEL DX D (IS=800.0E-18)
.MODEL QX NPN (IS=800.0E-18 BF=132)
.ENDS
*ALIAS V(24)=VOUT
*ALIAS V(36)=VIN-

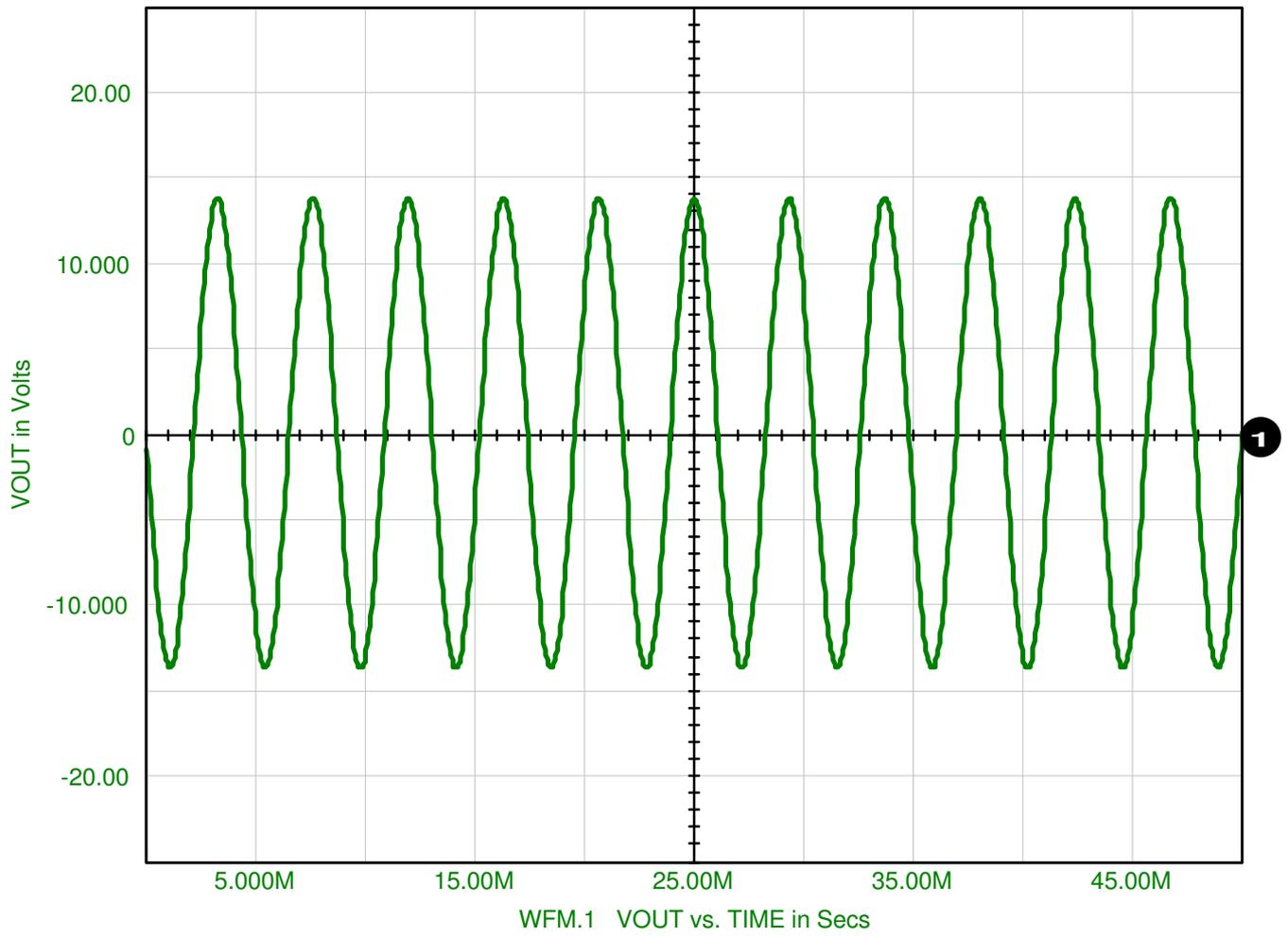
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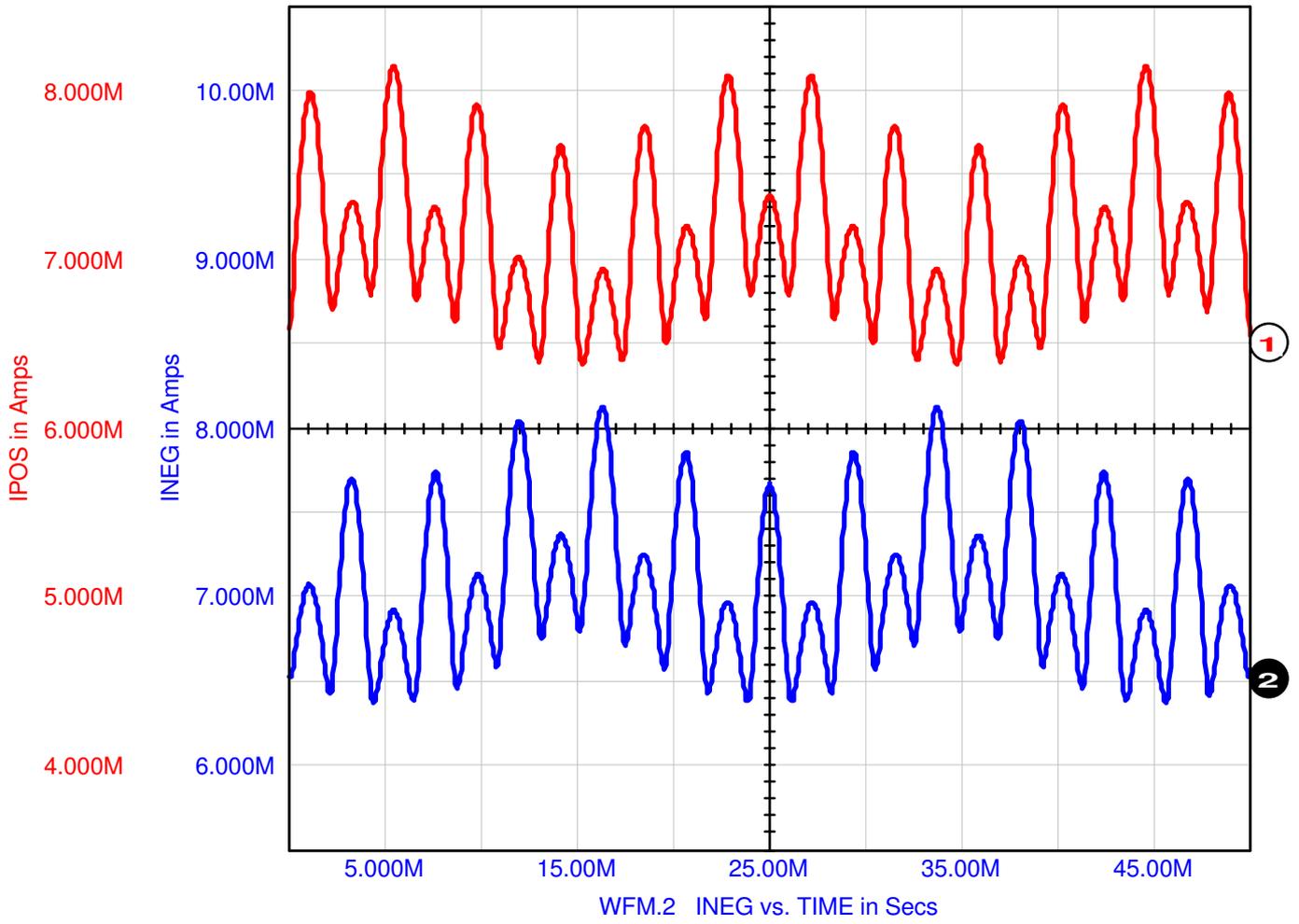
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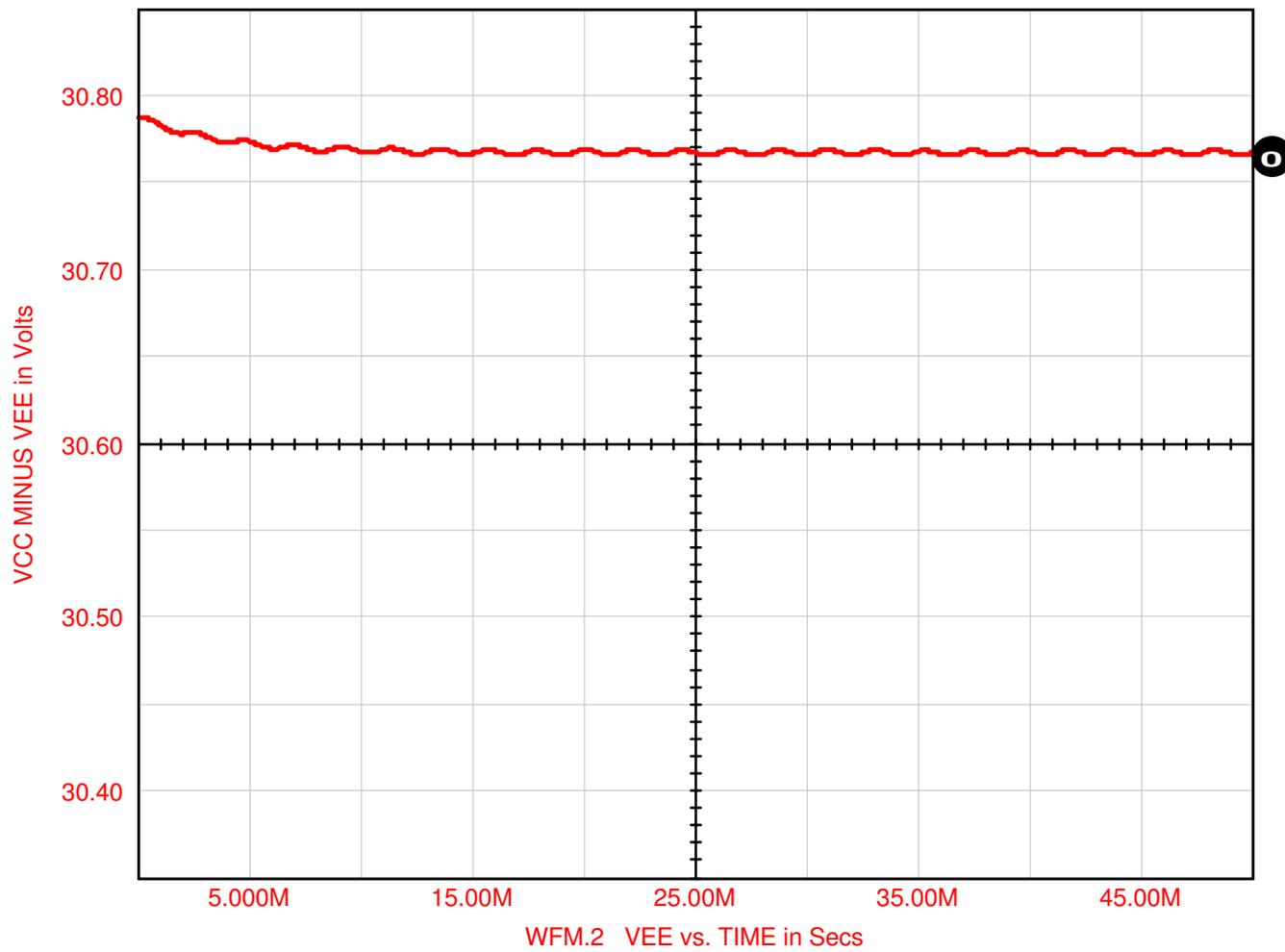
*ALIAS V(11)=VIN+
*ALIAS V(32)=VX1
*ALIAS V(12)=VX2
*ALIAS I(V103)=IVCC
*ALIAS I(V104)=IVEE
*ALIAS V(33)=VCC
*ALIAS V(14)=VEE
*ALIAS V(20)=VMC
*ALIAS I(V105)=IMC
*ALIAS I(V106)=INEG
*ALIAS I(V107)=IPOS
.PRINT TRAN V(24) V(36) V(11) V(32)
.PRINT TRAN V(12) I(V103) I(V104) V(33)
.PRINT TRAN V(14) V(20) I(V105) I(V106)
.PRINT TRAN I(V107)
R1 32 1 12K
R2 12 2 12K
V1 22 0 18
V2 0 23 18
R3 1 24 6K
R4 2 0 6K
V100 7 0 SIN 0 4.25 50
V101 8 9 SIN 0 13.76 230
V102 9 10 SIN 0 13.76 230
R100 9 7 10
R101 8 36 300
R102 10 11 300
R5 24 0 10K
X2 32 36 32 4 31 UA741
X3 12 11 12 4 31 UA741
V103 5 33
V104 14 27
Q1 17 17 26 QN2905
Q3 18 16 17 QN2905
Q2 16 17 26 QN2905
Q4 21 21 30 QN2222
Q5 29 21 30 QN2222
Q6 19 29 21 QN2222
R6 16 29 3.3K
C1 20 14 200U
D3 14 20 BZX79A15
C2 33 20 200U
D4 20 33 BZX79A15
R8 12 25 100K
R7 32 25 100K
D1 18 5 DN4148
D2 27 19 DN4148
X5 25 13 22 23 15 6 3 NE5534T
R9 15 13 1K
C3 6 3 22P
C4 25 0 100P
R10 0 20 10K
V105 15 20
V4 23 30 4
V3 26 22 4
V106 31 14
V107 33 4
X1 2 1 22 23 24 TL072T
.END

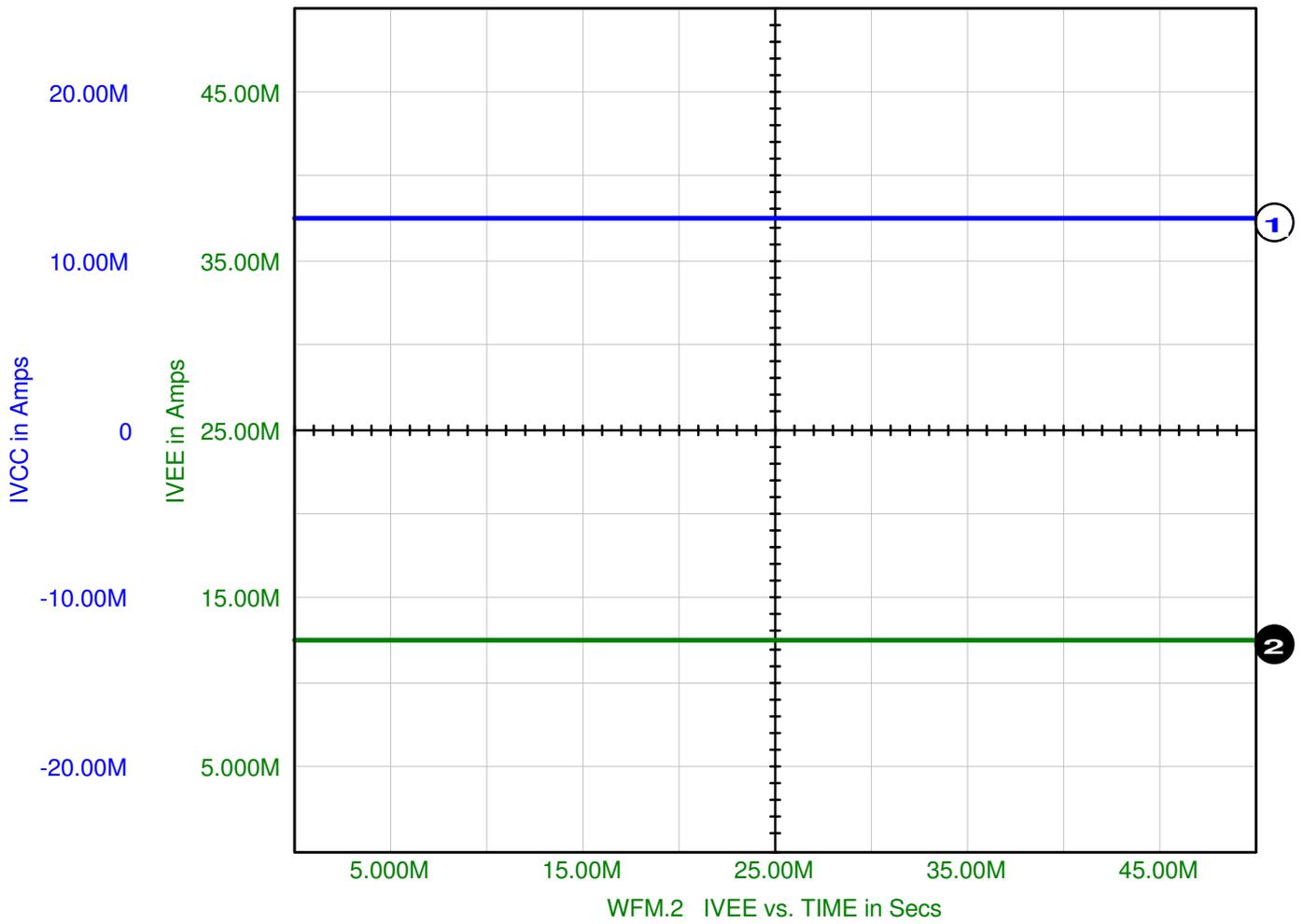
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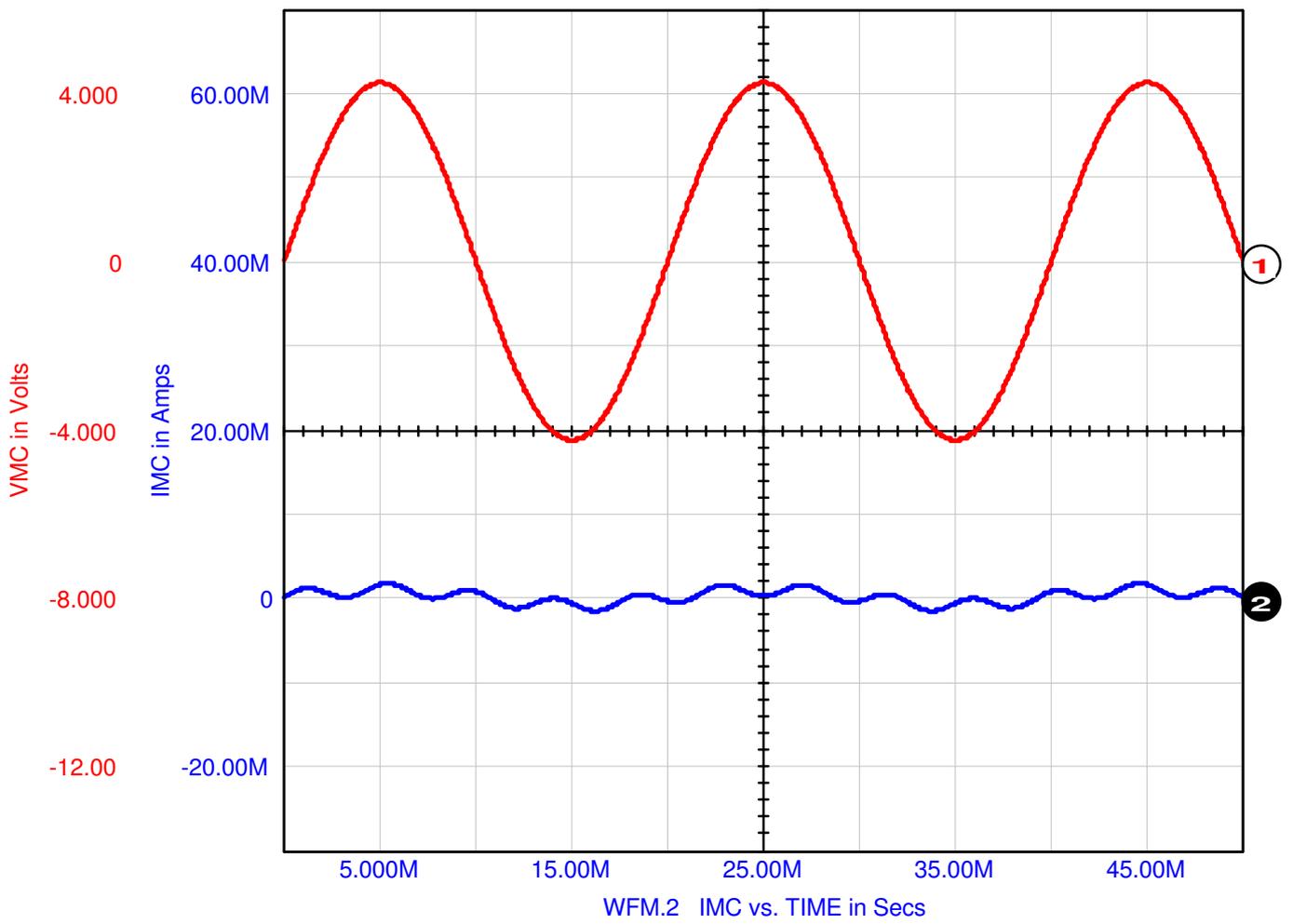








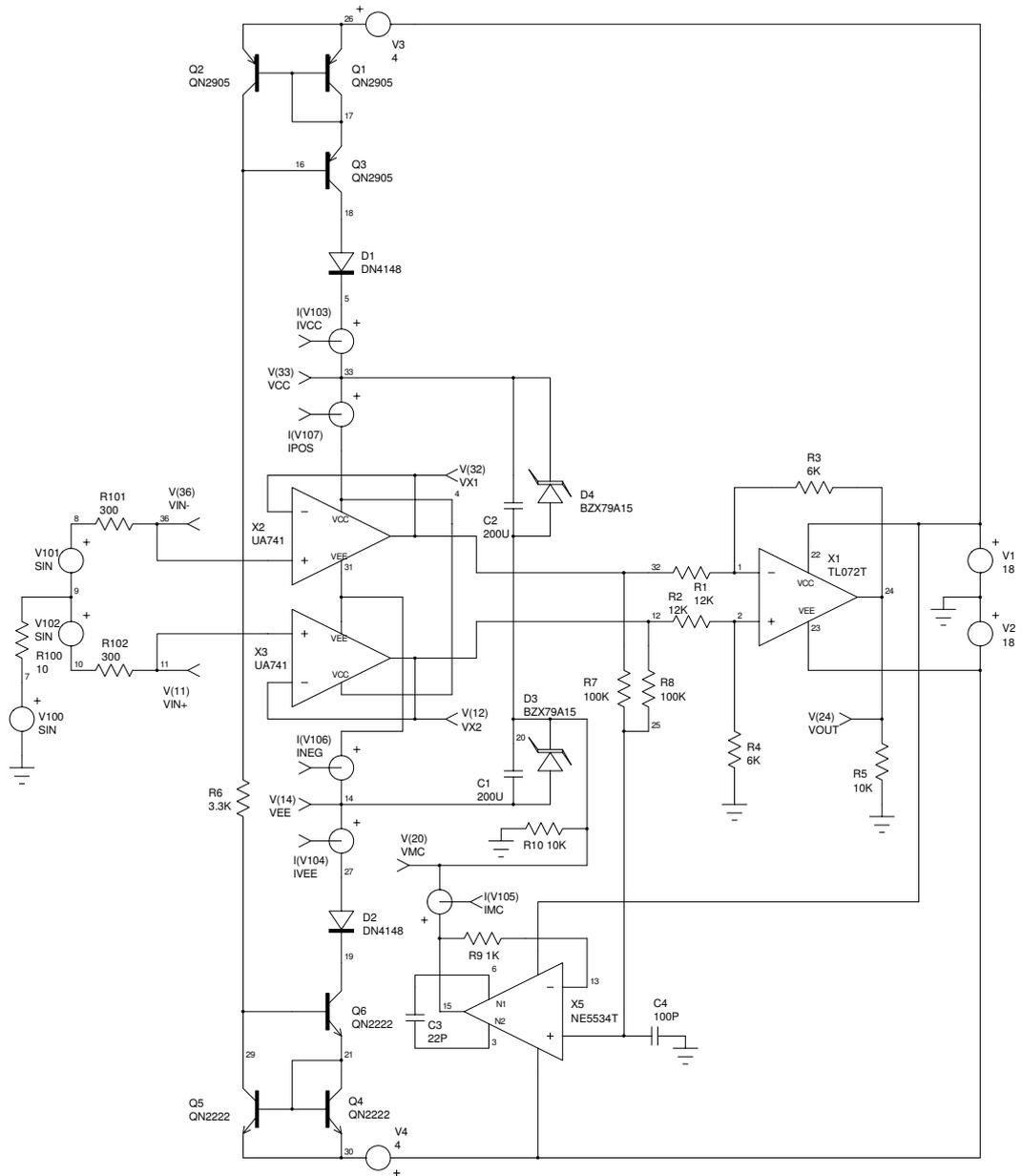




ANNEX B

SPICE simulation of a differential audio input amplifier

(simulation *input8.cir*)



INPUT 8

```

E:\SPICE4\NEXO\INPUT8
*SPICE_NET
*INCLUDE TIA.LIB
.SUBCKT TL072T      1 2 3 4 5
*
C1      11 12 3.498E-12
C2       6  7 15.00E-12
DC       5 53 DX
DE      54  5 DX
DLP     90 91 DX
DLN     92 90 DX
DP       4  3 DX
EGND   99  0 POLY(2) 3 0 4 0 0 .5 .5
FB      7 99 POLY(5) VB VC VE VLP VLN 0 4.715E6 -5E6 5E6 5E6 -5E6
GA      6  0 11 12 282.8E-6
GCM     0  6 10 99 8.942E-9
ISS     3 10 DC 195.0E-6
HLIM   90  0 VLIM 1K
J1     11  2 10 JX
J2     12  1 10 JX
R2      6  9 100.0E3
RD1     4 11 3.536E3
RD2     4 12 3.536E3
RO1     8  5 150
RO2     7 99 150
RP      3  4 2.143E3
RSS    10 99 1.026E6
VB      9  0 DC 0
VC      3 53 DC 2.200
VE     54  4 DC 2.200
VLIM    7  8 DC 0
VLP    91  0 DC 25
VLN     0 92 DC 25
.MODEL DX D(IS=800.0E-18)
.MODEL JX PJF(IS=15.00E-12 BETA=270.1E-6 VTO=-1)
.ENDS
.TRAN 50U 50M 0 50U
*INCLUDE NONLIN.LIB
.SUBCKT UA741 2      3 6 7 4
*
      - IN + OUT VCC VEE
*
QNI1 10 2 13 QNI1
QNI2 12 3 13 QNI2
.MODEL QNI1 NPN(NF=1.5 BF=111 IS=8E-16 CJE=3PF)
.MODEL QNI2 NPN(NF=1.5 BF=144 IS=8.3E-16 CJE=3PF)
Q3 13 14 4 QN741
IEE 4 14 185NA
CCM 13 4 2.5PF
RCM 13 4 10MEG
RC1 11 10 1K
RC2 11 12 1K
CHF 10 12 55PF
D1  7 11 D741
RP  7  4 10K
GA  0 15 12 10 .9MMHO
GCM 0 15 13 0 6.3NMHOS
R2  15 0 100K
D2  15 0 D741
D3  0 15 D741
C2  15 16 30PF
GB  16 0 15 0 12.5
RO2 16 0 1000
D4  16 17 D741P
EP  17 0 7 0 -1.8 1
D5  18 16 D741P
EN  0 18 0 4 -2.3 1
.MODEL D741P D(RS=1M)

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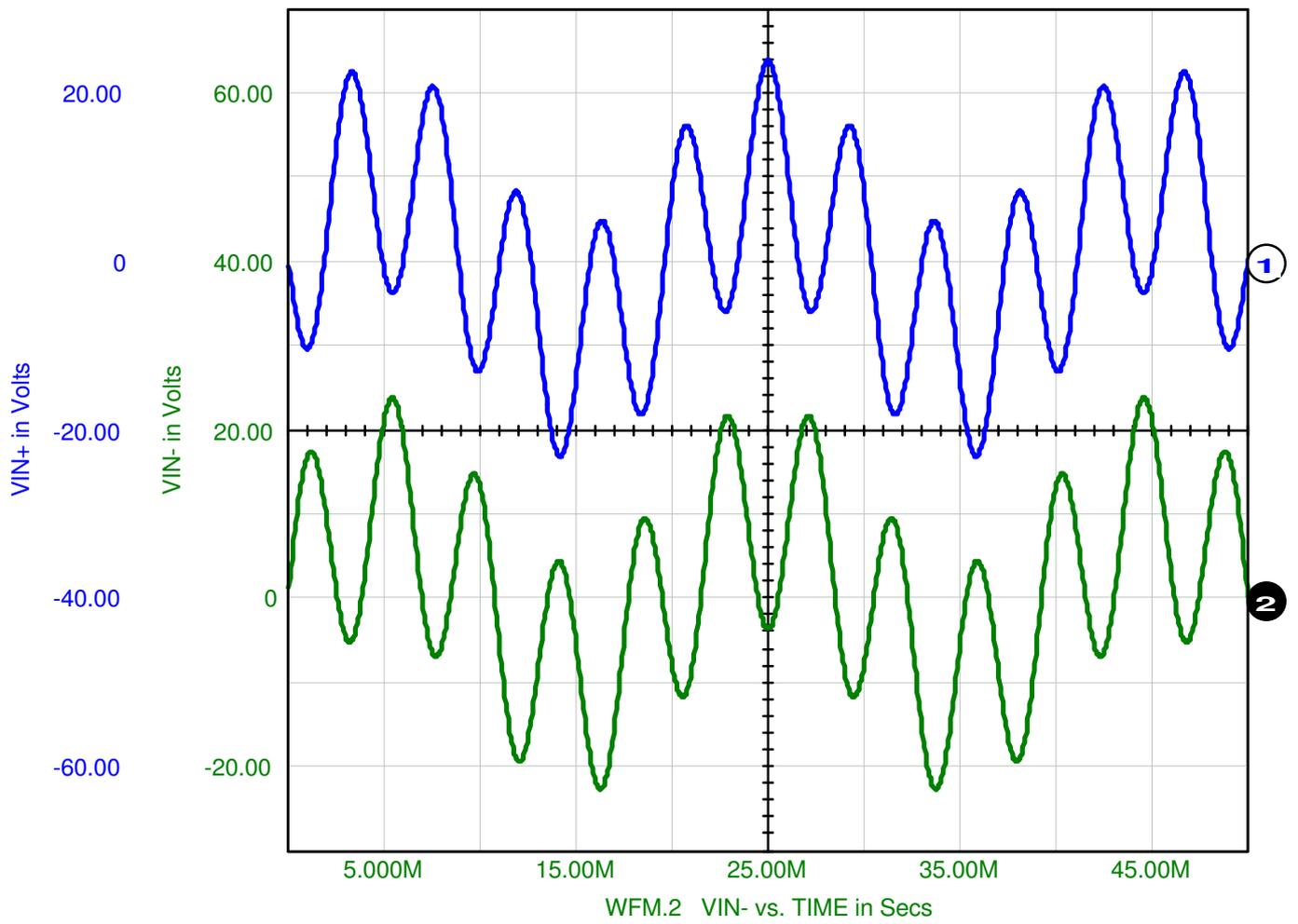
D6 19 16 D741
D7 16 20 D741
IRO 20 19 170UA
RR0 16 21 1MEG
Q4 7 19 21 QNO
Q5 4 20 21 QPO
.MODEL QNO NPN(BF=150 CJC=3P IS=1E-14)
.MODEL QPO PNP(BF=150 CJC=3P IS=1E-14)
L1 21 6 30UHY
RL1 21 6 1K
.MODEL D741 D(CJO=3PF)
.MODEL QN741 NPN
.ENDS
*INCLUDE BJTP.LIB
.MODEL QN2905 PNP (IS=3.81E-13 NF=1.0 BF=260 VAF=114
+ IKF=3.6E-01 ISE=5.85E-11 NE=2.0 BR=4 NR=1.0 VAR=20
+ XTB=1.5 RE=1.2E+00 RB=4.8E+00 RC=4.8E-01
+ CJE=4.6E-11 CJC=1.9E-11 TF=7.9E-10 TR=2.1E-08)
* 40 VOLT 0.60 AMP 200 MHZ SIPNP TRANSISTOR 08-06-1990
*INCLUDE DEVICE.LIB
.MODEL DN4148 D(RS=.8 CJO=4PF IS=7E-09 N=2 VJ=.6V
+ TT=6E-09 M=.45 BV=100V)
.MODEL QN2222 NPN(IS=1.9E-14 BF=150 VAF=100 IKF=.175 ISE=5E-11 NE=2.5
+ BR=7.5 VAR=6.38 IKR=.012 ISC=1.9E-13 NC=1.2 RC=.4 XTB=1.5
+ CJE=26PF TF=.5E-9 CJC=11PF TR=30E-9 KF=3.2E-16 AF=1.0)
*INCLUDE DIODE.LIB
.MODEL BZX79A15 D(RS=8.7297 BV=14.927
+ CJO=578.05P TT=20N N=2 IS=3.8E-09 IBV=1M)
* PHILIPS 15 VOLT ZENER
.OPTION ITL1=1000 METHOD=GEAR
*INCLUDE TI.LIB
.SUBCKT NE5534T 1 2 3 4 5 6 7
*
C1 11 12 7.703E-12
DC 5 53 DX
DE 54 5 DX
DLP 90 91 DX
DLN 92 90 DX
DP 4 3 DX
EGND 99 0 POLY(2) 3 0 4 0 0 .5 .5
FB 7 99 POLY(5) VB VC VE VLP VLN 0 2.893E6 -3E6 3E6 3E6 -3E6
GA 6 0 11 12 1.382E-3
GCM 0 6 10 99 13.82E-9
IEE 10 4 DC 133.0E-6
HLIM 90 0 VLIM 1K
Q1 11 2 13 QX
Q2 12 1 14 QX
R2 6 9 100.0E3
RC1 3 11 723.3
RC2 3 12 723.3
RE1 13 10 329
RE2 14 10 329
REE 10 99 1.504E6
RO1 8 5 50
RO2 7 99 25
RP 3 4 7.757E3
VB 9 0 DC 0
VC 3 53 DC 2.700
VE 54 4 DC 2.700
VLIM 7 8 DC 0
VLP 91 0 DC 38
VLN 0 92 DC 38
.MODEL DX D(IS=800.0E-18)
.MODEL QX NPN(IS=800.0E-18 BF=132)
.ENDS
*ALIAS V(24)=VOUT
*ALIAS V(36)=VIN-

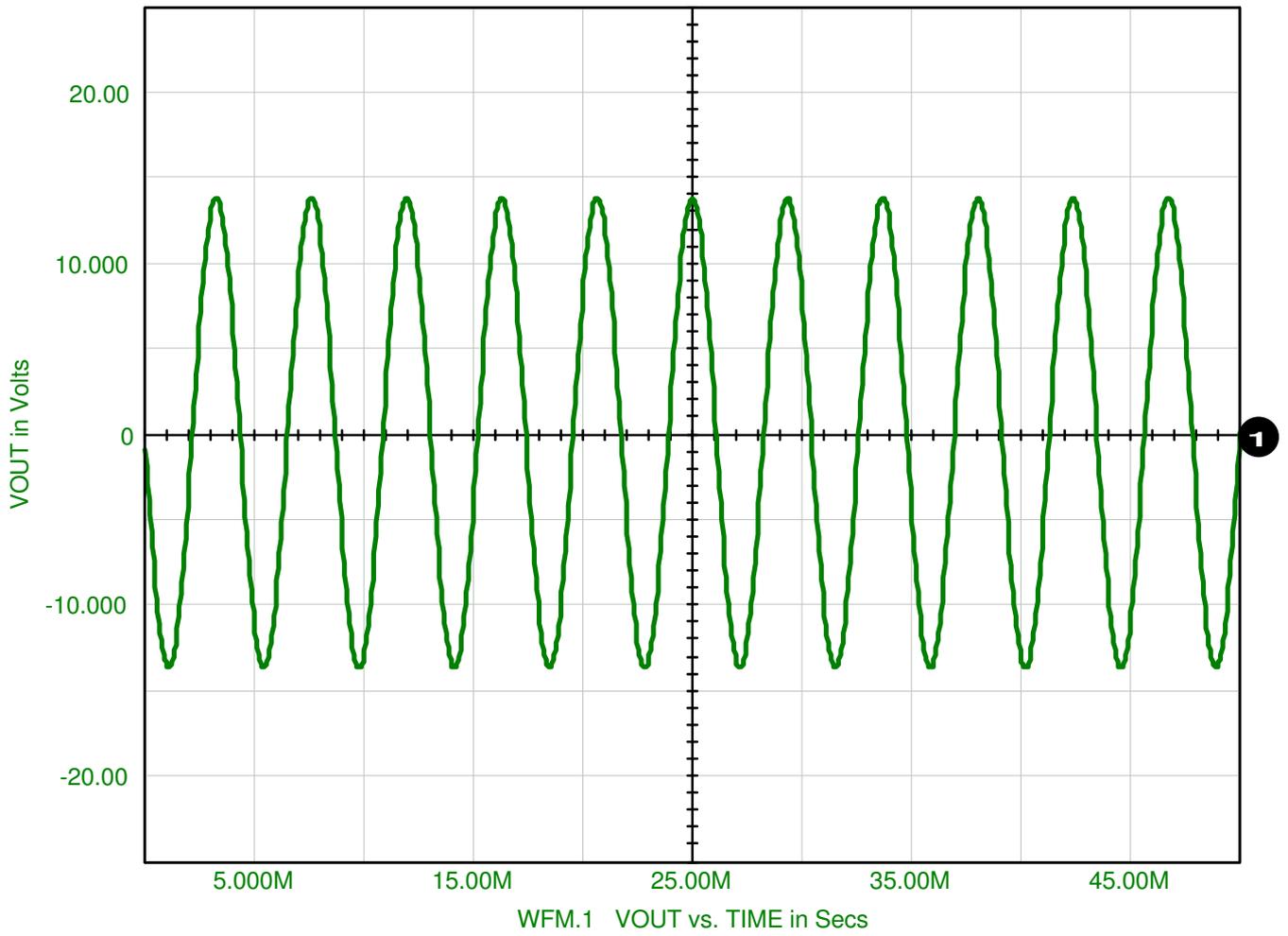
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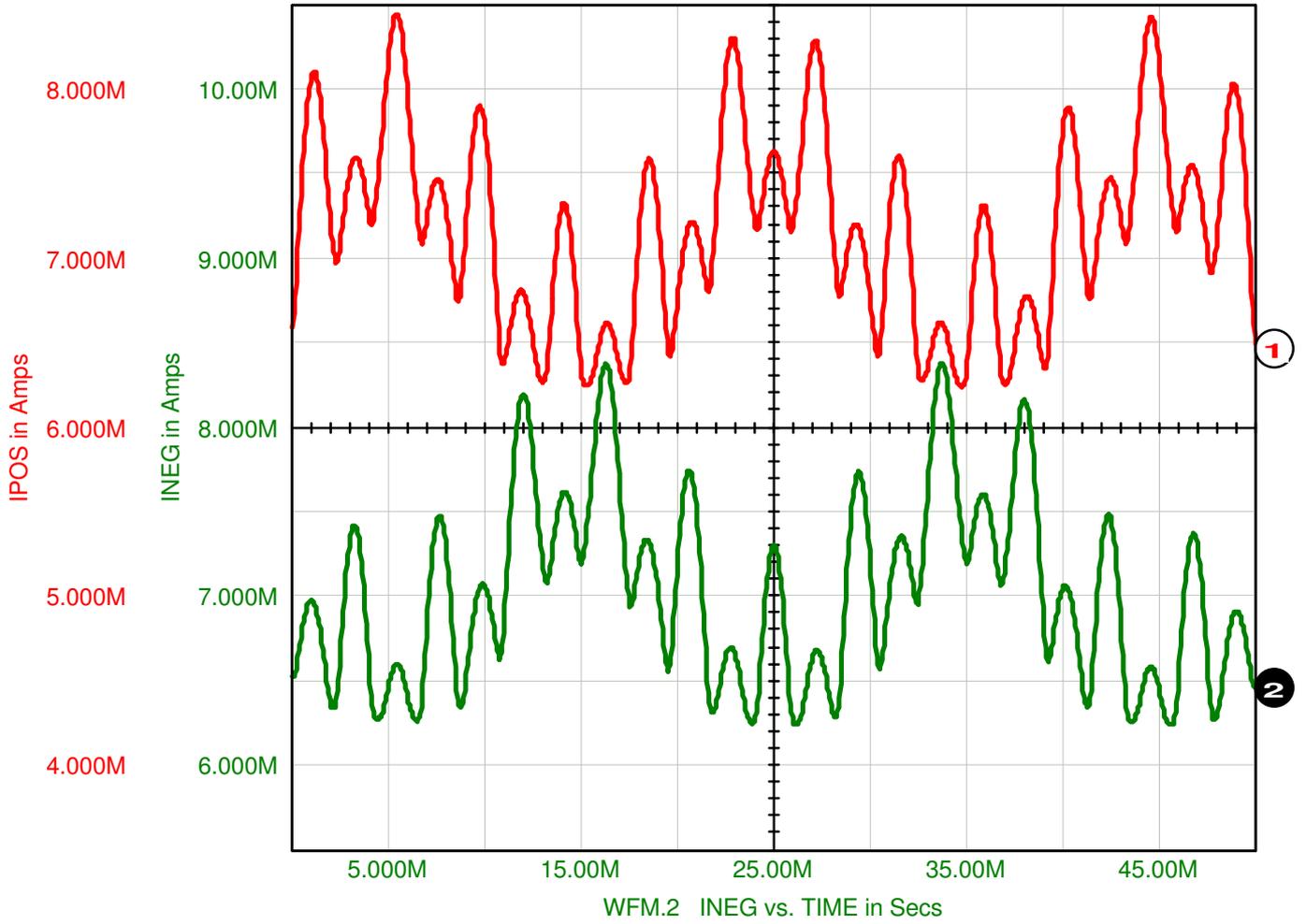
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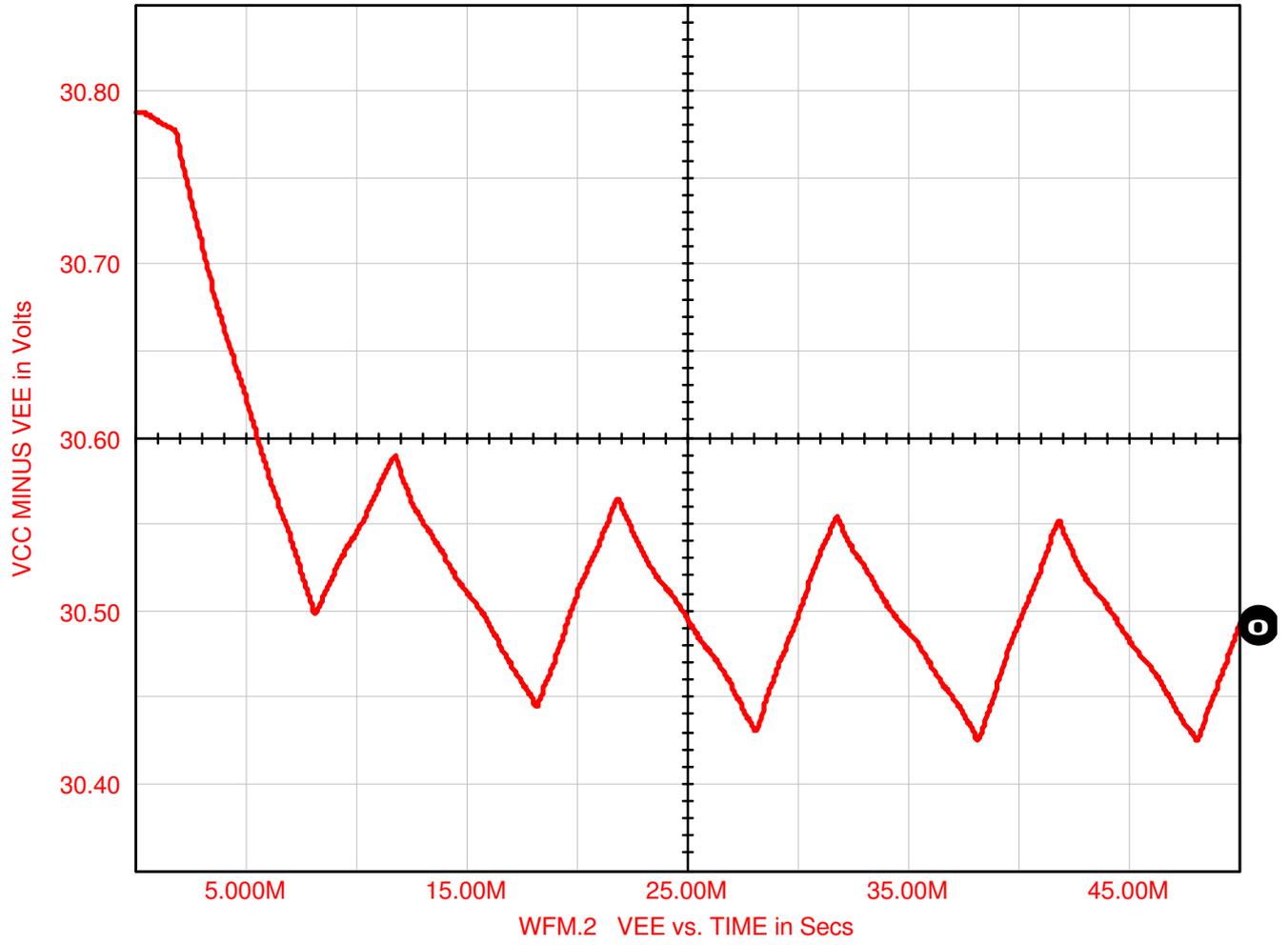
*ALIAS  V(11)=VIN+
*ALIAS  V(32)=VX1
*ALIAS  V(12)=VX2
*ALIAS  I(V103)=IVCC
*ALIAS  I(V104)=IVEE
*ALIAS  V(33)=VCC
*ALIAS  V(14)=VEE
*ALIAS  V(20)=VMC
*ALIAS  I(V105)=IMC
*ALIAS  I(V106)=INEG
*ALIAS  I(V107)=IPOS
.PRINT  TRAN  V(24)  V(36)  V(11)  V(32)
.PRINT  TRAN  V(12)  I(V103) I(V104) V(33)
.PRINT  TRAN  V(14)  V(20)  I(V105) I(V106)
.PRINT  TRAN  I(V107)
R1 32 1 12K
R2 12 2 12K
V1 22 0 18
V2 0 23 18
R3 1 24 6K
R4 2 0 6K
V100 7 0 SIN 0 9.90 50
V101 8 9 SIN 0 13.76 230
V102 9 10 SIN 0 13.76 230
R100 9 7 10
R101 8 36 300
R102 10 11 300
R5 24 0 10K
X2 32 36 32 4 31 UA741
X3 12 11 12 4 31 UA741
V103 5 33
V104 14 27
Q1 17 17 26 QN2905
Q3 18 16 17 QN2905
Q2 16 17 26 QN2905
Q4 21 21 30 QN2222
Q5 29 21 30 QN2222
Q6 19 29 21 QN2222
R6 16 29 3.3K
C1 20 14 200U
D3 14 20 BZX79A15
C2 33 20 200U
D4 20 33 BZX79A15
R8 12 25 100K
R7 32 25 100K
D1 18 5 DN4148
D2 27 19 DN4148
X5 25 13 22 23 15 6 3 NE5534T
R9 15 13 1K
C3 6 3 22P
C4 25 0 100P
R10 0 20 10K
V105 15 20
V4 23 30 4
V3 26 22 4
V106 31 14
V107 33 4
X1 2 1 22 23 24 TL072T
.END

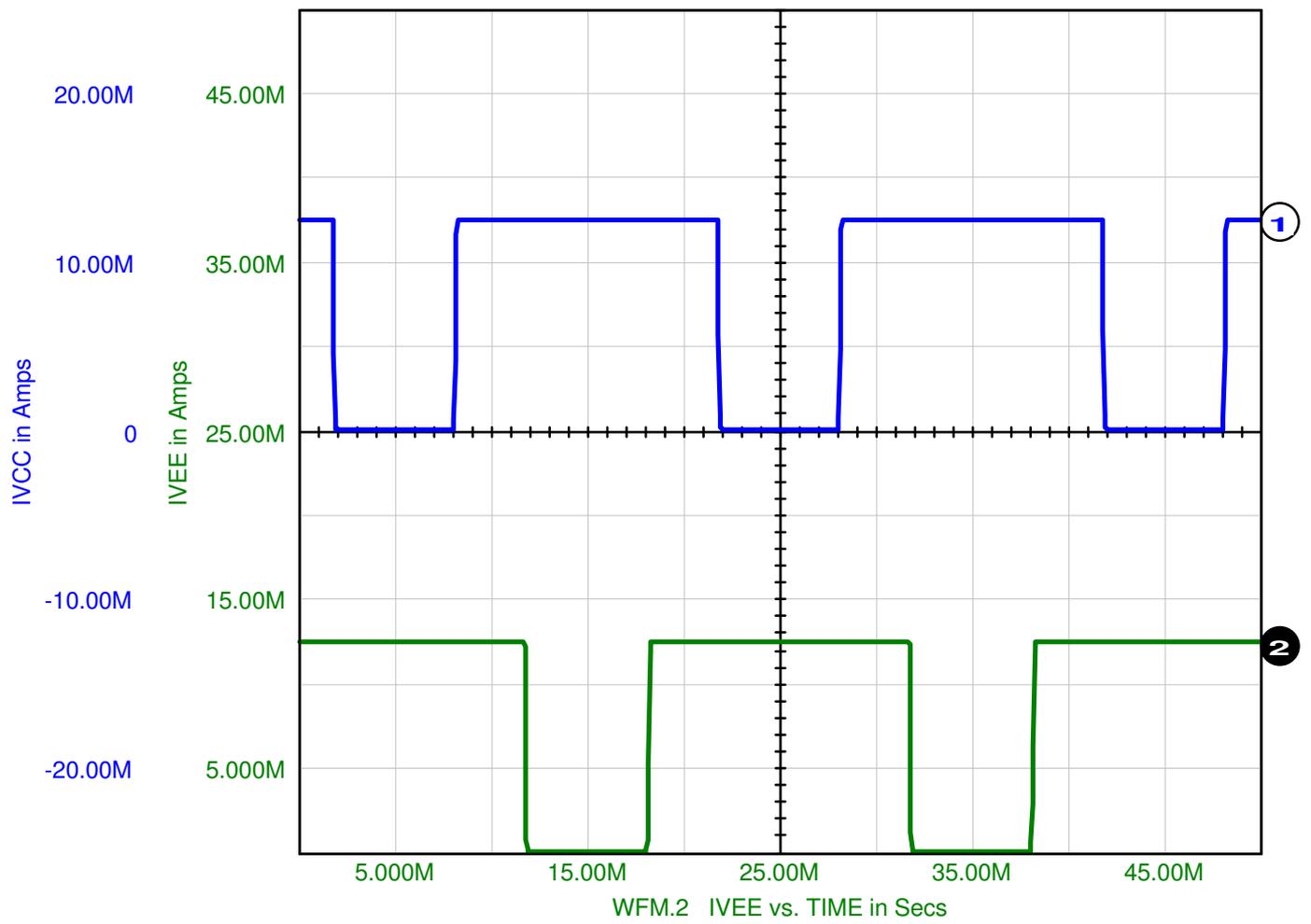
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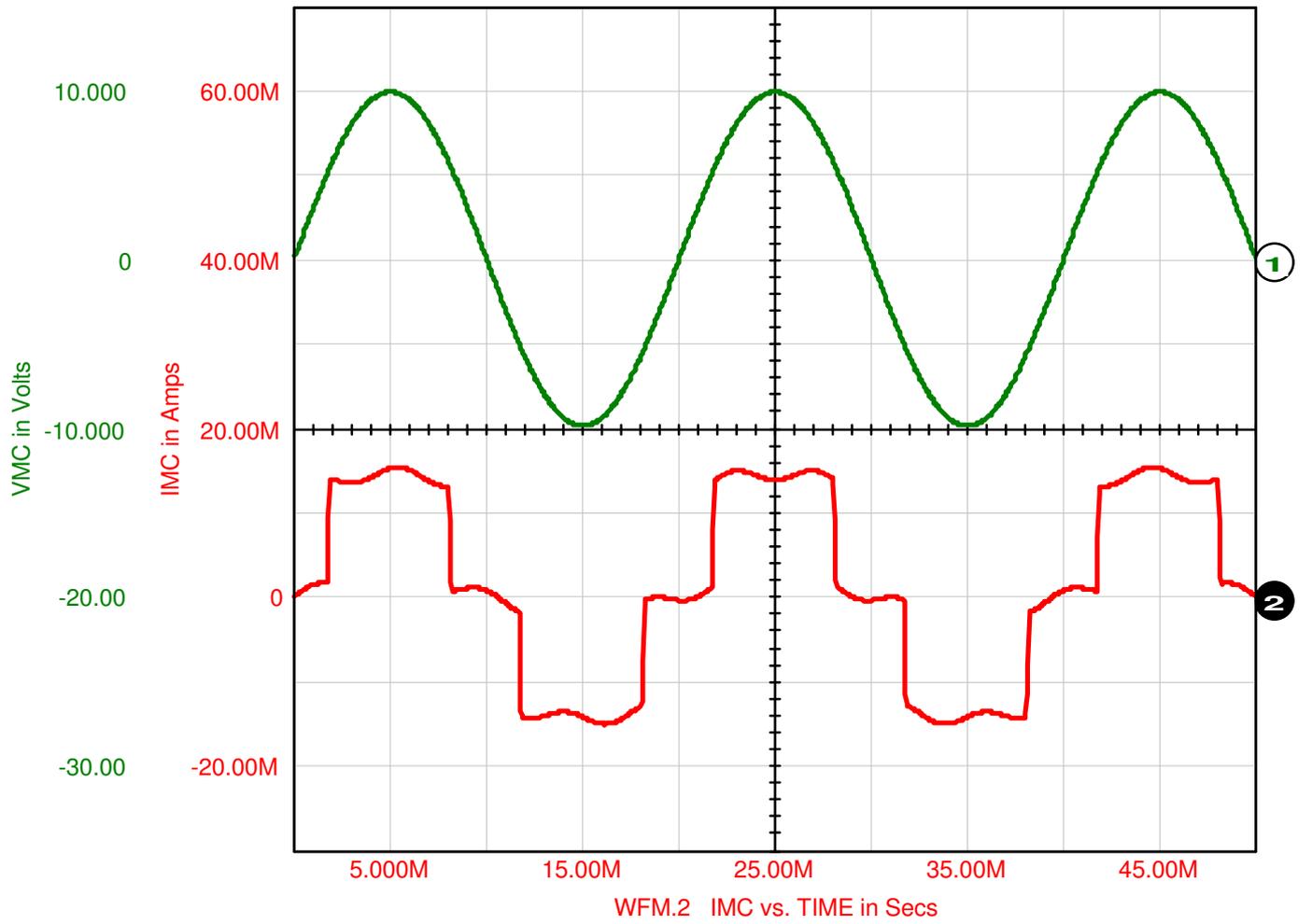






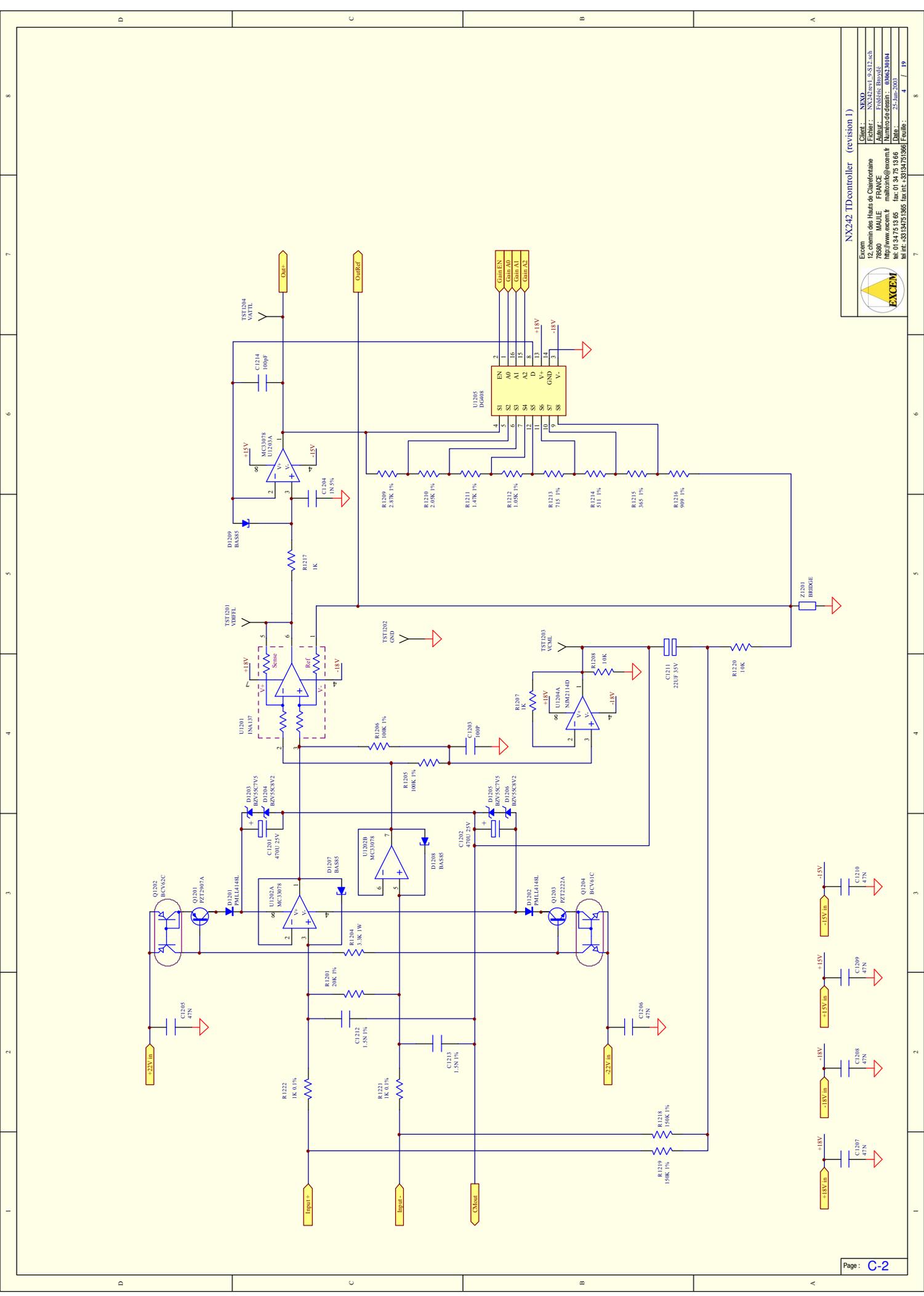






ANNEX C

Schematic diagram of an analog front-end of the NX242 TDcontroller



NX242 TDcontroller (revision 1)

Client : NIXO
 Fiche : NX242rev_1_012.sch
 Auteur : Frédéric Bravais
 Numéro de dessin : 00023014
 Date : 01/03/2010
 Rev : 01/03/2010
 Rev : 01/03/2010
 Rev : 01/03/2010

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